

May 2015

FQD3P50

P-Channel QFET® MOSFET

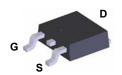
- 500 V, - 2.1 A, 4.9 Ω

Description

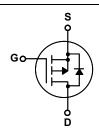
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 2.1 A, 500 V, $R_{DS(on)}$ = 4.9 Ω (Max.) @ V_{GS} = 10 V, ID = 1.05 A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 9.5 pF)
- · 100% Avalanche Tested



D-PAK (TO252)



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQD3P50	Unit
V _{DSS}	Drain-Source Voltage		-500	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		-2.1	Α
			-1.33	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	-8.4	Α
V_{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	250	mJ
I _{AR}	Avalanche Current	(Note 1)	-2.1	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-4.5	V/ns
P _D	Power Dissipation (T _A = 25°C) *		2.5	W
	Power Dissipation (T _C = 25°C)		50	W
	- Derate above 25°C		0.4	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

* When mounted on the minimum pad size recommended (PCB Mount)

Symbol	Parameter	FQD3P50	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. *	50	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-500			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		0.42		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -500 V, V _{GS} = 0 V			-1	μА
		V _{DS} = -400 V, T _C = 125°C			-10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	Gate-Body Leakage Current, Forward V _{GS} = -30 V, V _{DS} = 0 V		-	-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse V _{GS} = 30 V, V _{DS} = 0 V			-	100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage				-5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -1.05 A		3.9	4.9	Ω
9 _{FS}	Forward Transconductance	V _{DS} = -50 V, I _D = -1.05 A		2.1		S
C _{iss} C _{oss}	Output Capacitance Reverse Transfer Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		70 9.5	90 12	pF pF
C _{rss}	Reverse Transfer Capacitance					pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = -250 V, I _D = -2.7 A,		12	35	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		56	120	ns
t _{d(off)}	Turn-Off Delay Time			35	80	ns
	T 000 T 11 T	(Note 4)		45	100	ns
t _f	Turn-Off Fall Time	(**************************************				
•	Total Gate Charge	, ,		18	23	nC
•		V _{DS} = -400 V, I _D = -2.7 A, V _{GS} = -10 V		18 3.6	23	
	Total Gate Charge	V _{DS} = -400 V, I _D = -2.7 A,				nC
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge	V_{DS} = -400 V, I_{D} = -2.7 A, V_{GS} = -10 V (Note 4)		3.6		nC nC
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DS} = -400 V, I_{D} = -2.7 A, V_{GS} = -10 V (Note 4)		3.6		nC
Q_g Q_{gs} Q_{gd} Drain-S	Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics ar	V _{DS} = -400 V, I _D = -2.7 A, V _{GS} = -10 V (Note 4) Maximum Ratings de Forward Current Forward Current		3.6		nC nC
Q_g Q_{gs} Q_{gd} Drain-S Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics and Maximum Continuous Drain-Source Diode	V_{DS} = -400 V, I_{D} = -2.7 A, V_{GS} = -10 V (Note 4) and Maximum Ratings ode Forward Current Forward Current V_{GS} = 0 V, I_{S} = -2.1 A		3.6	-2.1	nC nC
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge Source Diode Characteristics ar Maximum Continuous Drain-Source Diode Maximum Pulsed Drain-Source Diode F	V _{DS} = -400 V, I _D = -2.7 A, V _{GS} = -10 V (Note 4) Maximum Ratings de Forward Current Forward Current		3.6 9.2	-2.1 -8.4	nC nC

Notes:1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 102mH, I_{AS} = -2.1A, V_{DD} = -50V, R_G = 25 Ω , Starting T_J = 25°C 3. $I_{SD} \le$ -2.7A, di/dt \le 200A/ μ s, $V_{DD} \le$ BV $_{DSS}$, Starting T_J = 25°C 4. Essentially independent of operating temperature

Typical Characteristics

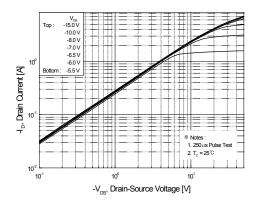


Figure 1. On-Region Characteristics

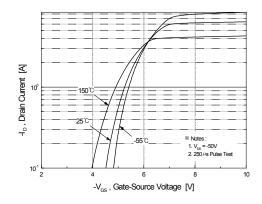


Figure 2. Transfer Characteristics

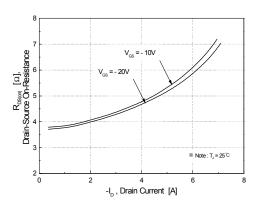


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

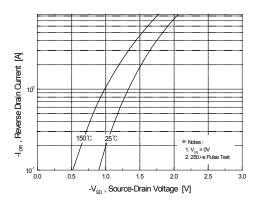


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

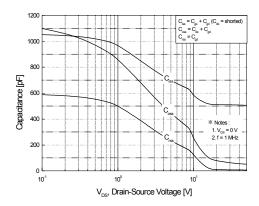


Figure 5. Capacitance Characteristics

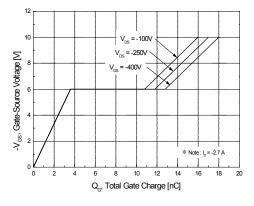


Figure 6. Gate Charge Characteristics

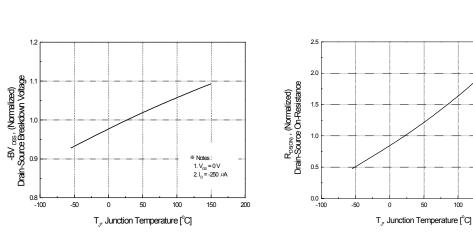


Figure 7. Breakdown Voltage Variation vs. Temperature

Typical Characteristics (Continued)

Figure 8. On-Resistance Variation vs. Temperature

1. V_{GS} = -10 V 2. I_D = -1.35 A

150

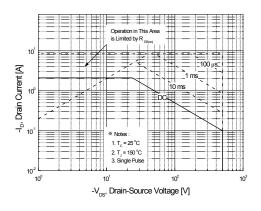


Figure 9. Maximum Safe Operating Area

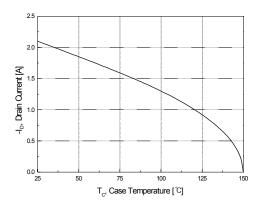


Figure 10. Maximum Drain Current vs. Case Temperature

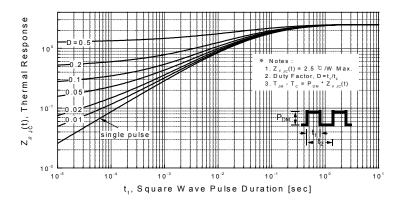
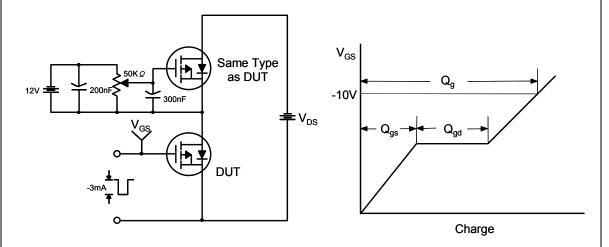
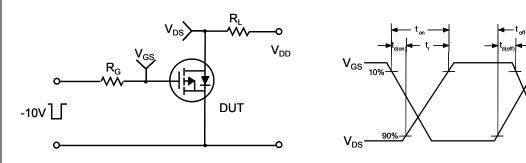


Figure 11. Transient Thermal Response Curve

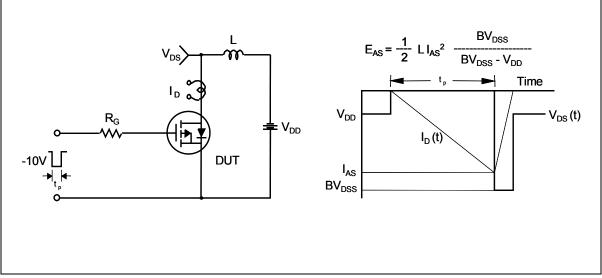
Gate Charge Test Circuit & Waveform



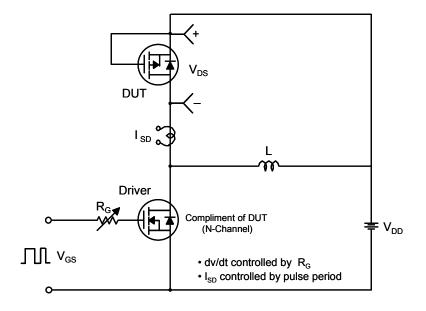
Resistive Switching Test Circuit & Waveforms

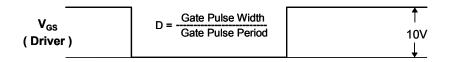


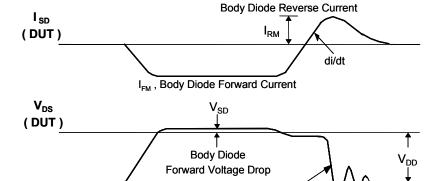
Unclamped Inductive Switching Test Circuit & Waveforms



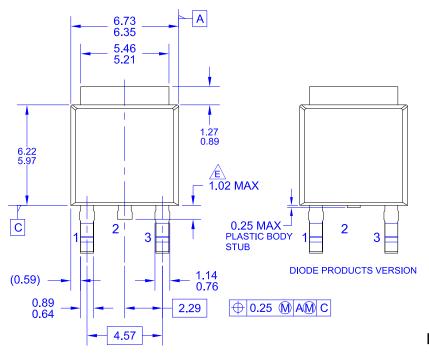
Peak Diode Recovery dv/dt Test Circuit & Waveforms

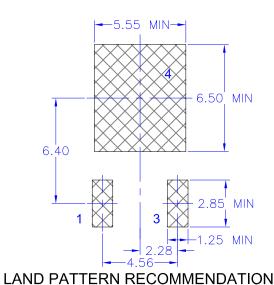




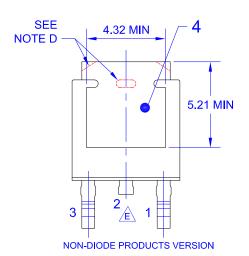


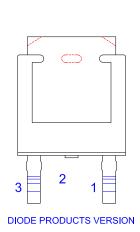
Body Diode Recovery dv/dt

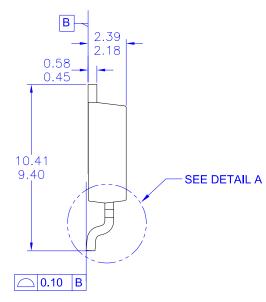




NON-DIODE PRODUCTS VERSION



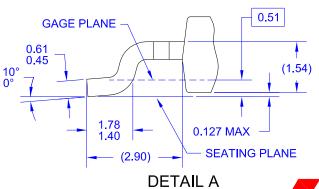




NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
- ISSUE C, VARIATION AA.

 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



(ROTATED -90°) SCALE: 12X







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Definition of Terms

Definition of Terms				
Datasheet Identification	Product Status	Definition		
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.		
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
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