

## LM13700/LM13700A Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

### General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of  $I_{ABC}$ . This may result in performance superior to that of the LM13600 in audio applications.

- Excellent  $g_m$  linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio

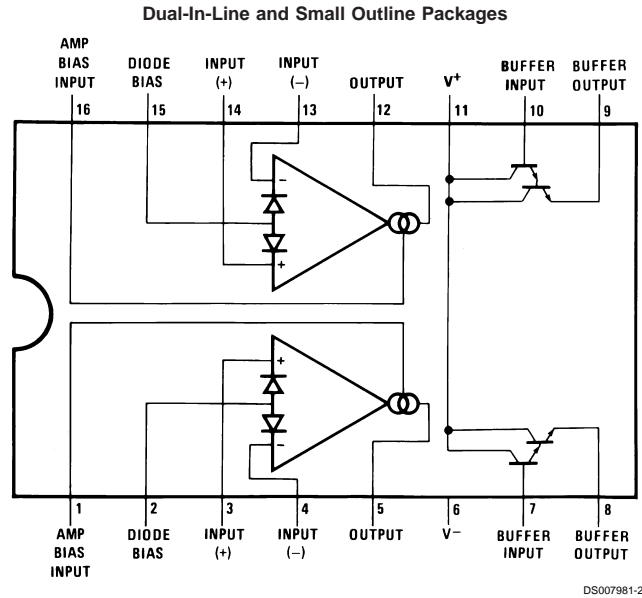
### Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

### Features

- $g_m$  adjustable over 6 decades

### Connection Diagram



Top View  
Order Number LM13700M, LM13700N or LM13700AN  
See NS Package Number M16A or N16A

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	
LM13700	36 V <sub>DC</sub> or ±18V
LM13700A	44 V <sub>DC</sub> or ±22V
Power Dissipation (Note 3) T <sub>A</sub> = 25°C	
LM13700N, LM13700AN	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I <sub>D</sub> )	2 mA
Amplifier Bias Current (I <sub>ABC</sub> )	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 4)	20 mA

## Operating Temperature Range

LM13700N, LM13700AN	0°C to +70°C
DC Input Voltage	+V <sub>S</sub> to -V <sub>S</sub>
Storage Temperature Range	-65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 5)

Parameter	Conditions	LM13700			LM13700A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V <sub>OS</sub> )			0.4	4		0.4	1	mV
	Over Specified Temperature Range I <sub>ABC</sub> = 5 μA		0.3	4		0.3	1	
V <sub>OS</sub> Including Diodes	Diode Bias Current (I <sub>D</sub> ) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I <sub>ABC</sub> ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current	Over Specified Temperature Range		0.4	5		0.4	5	μA
			1	8		1	7	
Forward Transconductance (g <sub>m</sub> )		6700	9600	13000	7700	9600	12000	μmho
g <sub>m</sub> Tracking	Over Specified Temperature Range	5400			4000			
Peak Output Current	R <sub>L</sub> = 0, I <sub>ABC</sub> = 5 μA		5		3	5	7	μA
	R <sub>L</sub> = 0, I <sub>ABC</sub> = 500 μA	350	500	650	350	500	650	
	R <sub>L</sub> = 0, Over Specified Temp Range	300			300			
Peak Output Voltage	Positive	R <sub>L</sub> = ∞, 5 μA ≤ I <sub>ABC</sub> ≤ 500 μA	+12	+14.2		+12	+14.2	V
	Negative	R <sub>L</sub> = ∞, 5 μA ≤ I <sub>ABC</sub> ≤ 500 μA	-12	-14.4		-12	-14.4	V
Supply Current	I <sub>ABC</sub> = 500 μA, Both Channels		2.6			2.6		mA
V <sub>OS</sub> Sensitivity	Positive	ΔV <sub>OS</sub> /ΔV <sup>+</sup>	20	150		20	150	μV/V
	Negative	ΔV <sub>OS</sub> /ΔV <sup>-</sup>	20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 6) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	I <sub>ABC</sub> = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	I <sub>ABC</sub> = 0 (Refer to Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		kΩ
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 6)		0.5	2		0.5	2	μA
Peak Buffer Output Voltage	(Note 6)	10			10			V

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

**Note 2:** For selections to a supply voltage above ±22V, contact factory.

## Electrical Characteristics (Note 5) (Continued)

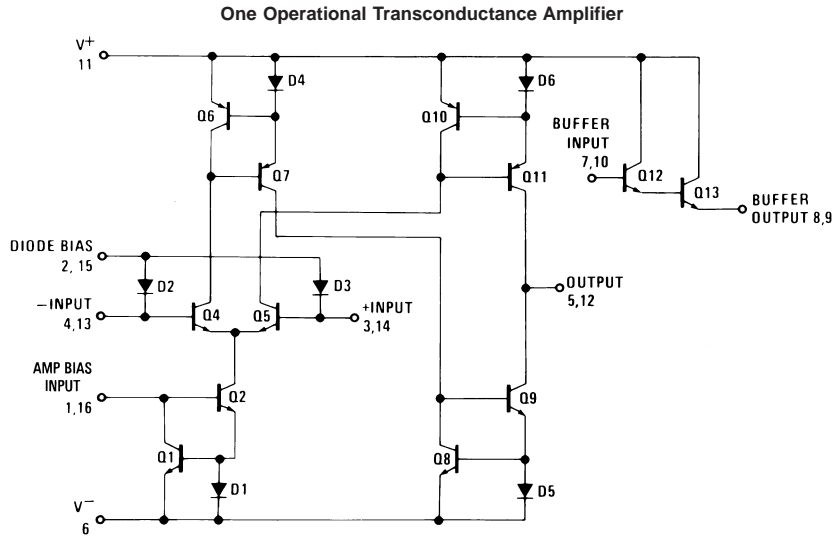
**Note 3:** For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W; LM13700M, 110°C/W.

**Note 4:** Buffer output current should be limited so as to not exceed package dissipation.

**Note 5:** These specifications apply for  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , amplifier bias current ( $I_{ABC}$ ) = 500  $\mu A$ , pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

**Note 6:** These specifications apply for  $V_S = \pm 15V$ ,  $I_{ABC} = 500 \mu A$ ,  $R_{OUT} = 5 k\Omega$  connected from the buffer output to  $-V_S$  and the input of the buffer is connected to the transconductance amplifier output.

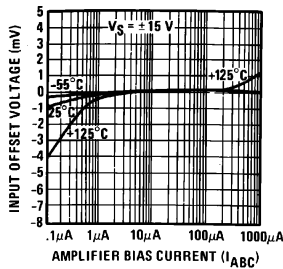
## Schematic Diagram



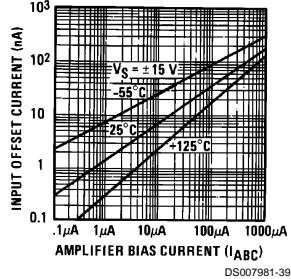
DS007981-1

## Typical Performance Characteristics

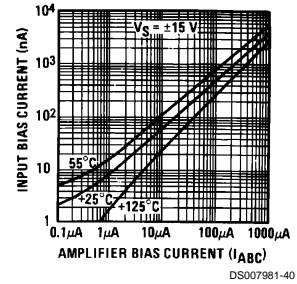
**Input Offset Voltage**



**Input Offset Current**

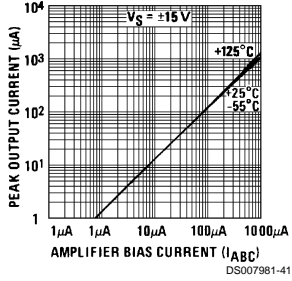


**Input Bias Current**



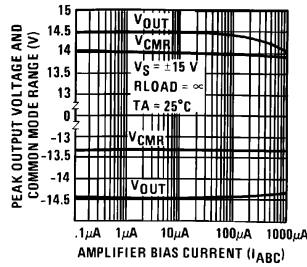
## Typical Performance Characteristics (Continued)

Peak Output Current



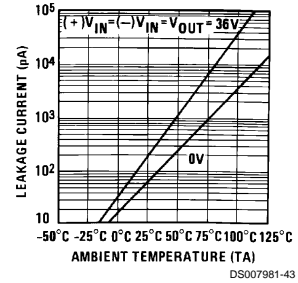
DS007981-41

Peak Output Voltage and Common Mode Range



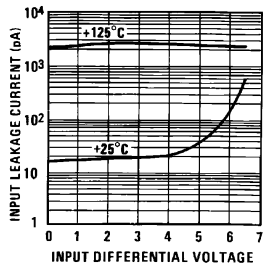
DS007981-42

Leakage Current



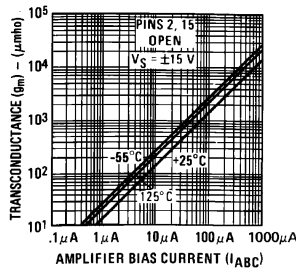
DS007981-43

Input Leakage



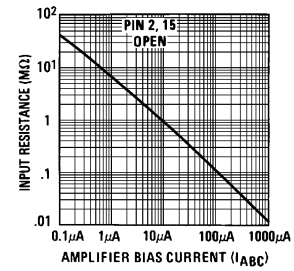
DS007981-44

Transconductance



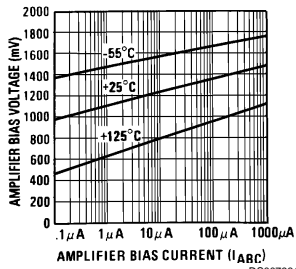
DS007981-45

Input Resistance



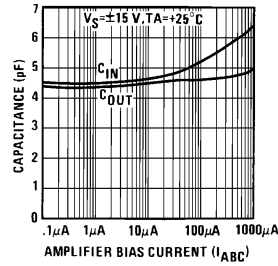
DS007981-46

Amplifier Bias Voltage vs Amplifier Bias Current



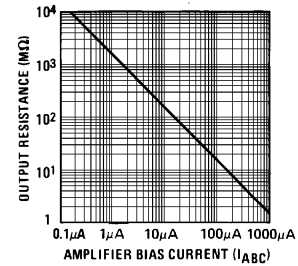
DS007981-47

Input and Output Capacitance



DS007981-48

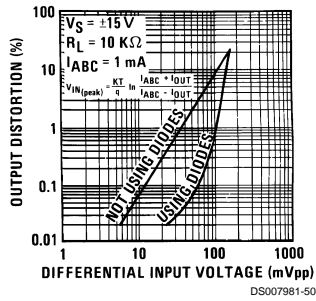
Output Resistance



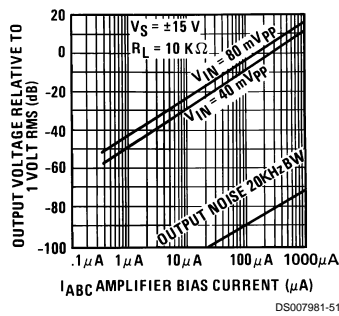
DS007981-49

## Typical Performance Characteristics (Continued)

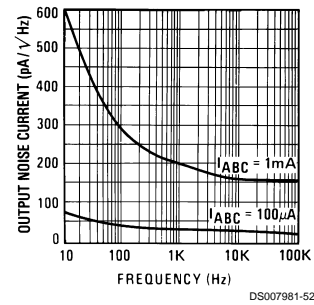
**Distortion vs Differential Input Voltage**



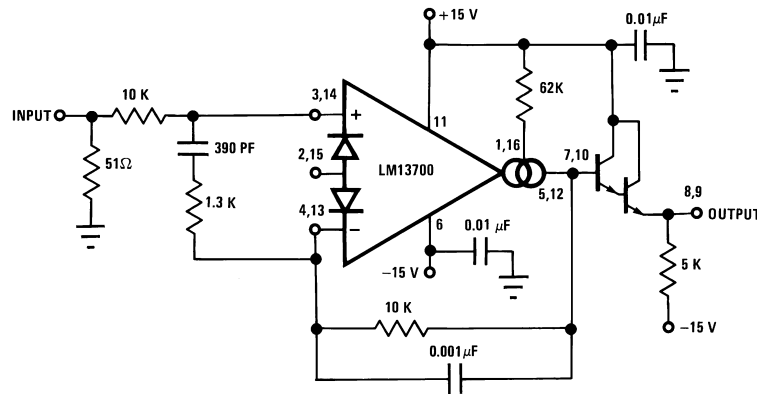
**Voltage vs Amplifier Bias Current**



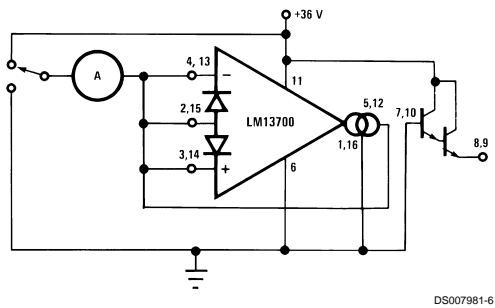
**Output Noise vs Frequency**



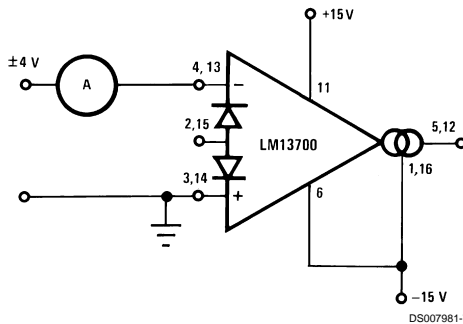
**Unity Gain Follower**



**Leakage Current Test Circuit**



**Differential Input Current Test Circuit**



## Circuit Description

The differential transistor pair  $Q_4$  and  $Q_5$  form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where  $V_{IN}$  is the differential input voltage,  $kT/q$  is approximately 26 mV at 25°C and  $I_5$  and  $I_4$  are the collector currents of transistors  $Q_5$  and  $Q_4$  respectively. With the exception of

## Circuit Description (Continued)

$Q_3$  and  $Q_{13}$ , all transistors and diodes are identical in size. Transistors  $Q_1$  and  $Q_2$  with Diode  $D_1$  form a current mirror which forces the sum of currents  $I_4$  and  $I_5$  to equal  $I_{ABC}$ :

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where  $I_{ABC}$  is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of  $I_4$  and  $I_5$  approaches unity and the Taylor series of the  $\ln$  function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4}$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2} \quad (3)$$

$$V_{IN} \left[ \frac{I_{ABC}^q}{2kT} \right] = I_5 - I_4 \quad (4)$$

Collector currents  $I_4$  and  $I_5$  are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to  $I_5$  minus  $I_4$  thus:

$$V_{IN} \left[ \frac{I_{ABC}^q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to  $I_{ABC}$ .

## Linearizing Diodes

For differential voltages greater than a few millivolts, Equation (3) becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the

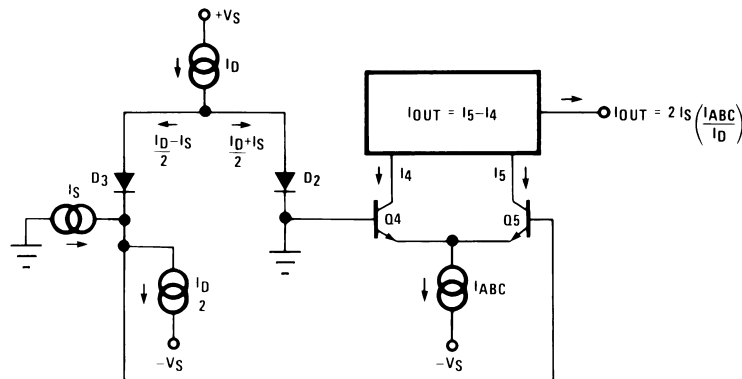


FIGURE 1. Linearizing Diodes

For optimum signal-to-noise performance,  $I_{ABC}$  should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of

amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current  $I_S$ . Since the sum of  $I_4$  and  $I_5$  is  $I_{ABC}$  and the difference is  $I_{OUT}$ , currents  $I_4$  and  $I_5$  can be written as follows:

$$I_4 = \frac{I_{ABC} - I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC} + I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC} + I_{OUT}}{2}}{\frac{I_{ABC} - I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S \left( \frac{2I_{ABC}}{I_D} \right) \text{ for } |I_S| < \frac{I_D}{2} \quad (6)$$

Notice that in deriving Equation (6) no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed  $I_D/2$  and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

## Applications: Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the  $13 \text{ k}\Omega$  resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

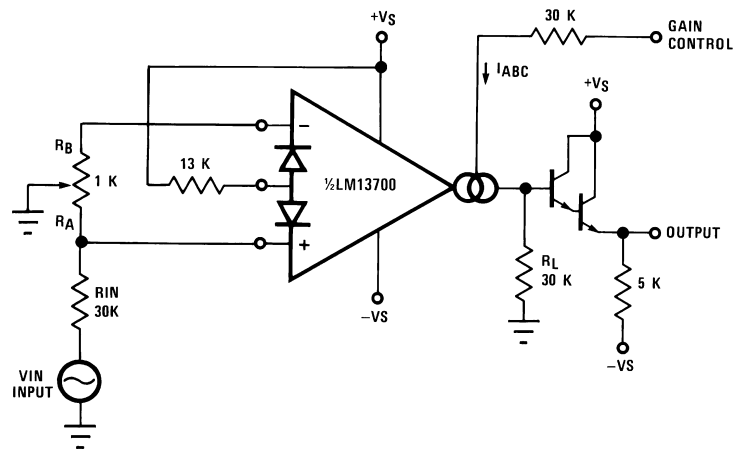
the input signal via  $R_{IN}$  (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting  $R_L$ .

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors,  $I_D$  should be as large as possible. This minimizes the dynamic junction resistance of the diodes ( $r_d$ ) and

## Applications: Voltage Controlled Amplifiers

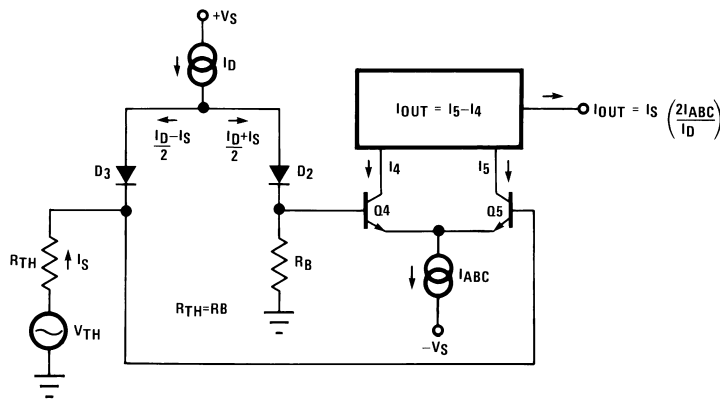
(Continued)

maximizes their linearizing action when balanced against  $R_{IN}$ . A value of 1 mA is recommended for  $I_D$  unless the specific application demands otherwise.



DS007981-9

FIGURE 2. Voltage Controlled Amplifier



DS007981-10

FIGURE 3. Equivalent VCA Input Circuit

## Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB.  $R_P$  is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If  $V_C$  is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D} (I_{ABC}) = \frac{-2I_S}{I_D} \frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D} \frac{(V^- + 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding  $I_S \times I_D R_C / 2(V^- + 1.4V)$  into  $I_O$ . The circuit of Figure 6 adds  $R_M$  to provide this current, resulting in a four-quadrant multiplier where  $R_C$  is trimmed such that  $V_O = 0V$  for  $V_{IN2} = 0V$ .  $R_M$  also serves as the load resistor for  $I_O$ .

## Stereo Volume Control (Continued)

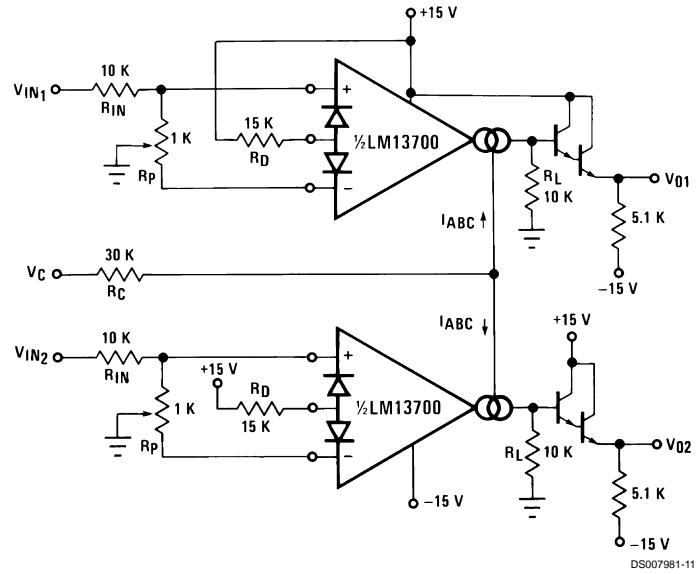


FIGURE 4. Stereo Volume Control

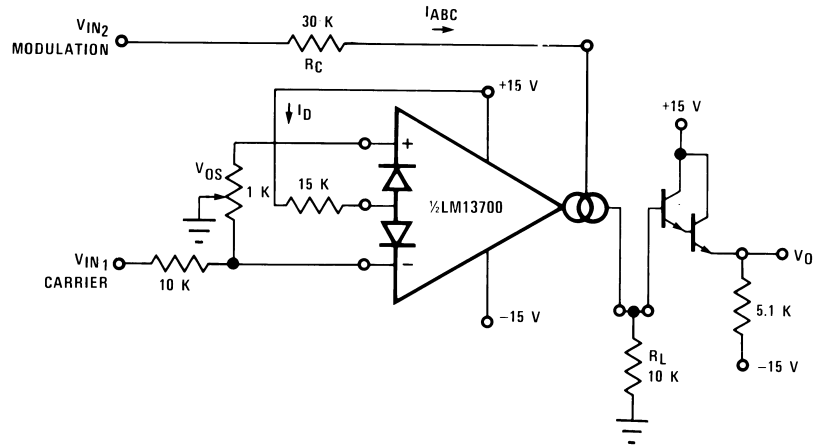


FIGURE 5. Amplitude Modulator



## Stereo Volume Control (Continued)

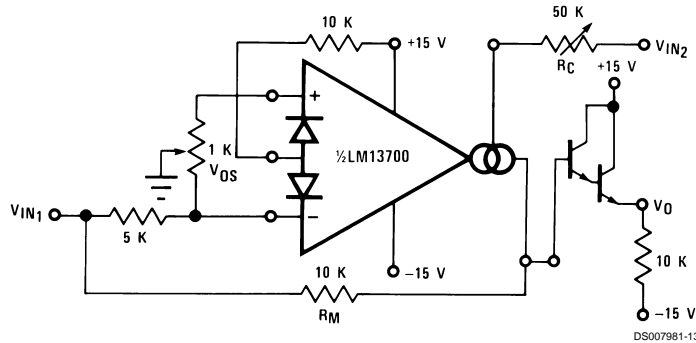


FIGURE 6. Four-Quadrant Multiplier

Noting that the gain of the LM13700 amplifier of Figure 3 may be controlled by varying the linearizing diode current  $I_D$  as well as by varying  $I_{ABC}$ , Figure 7 shows an AGC Amplifier using this approach. As  $V_O$  reaches a high enough amplitude ( $3V_{BE}$ ) to turn on the Darlingtons and the linearizing diodes, the increase in  $I_D$  reduces the amplifier gain so as to hold  $V_O$  at that level.

## Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at  $R_X$  generates a  $V_{IN}$  to the LM13700 which is then multiplied by the  $g_m$  of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where  $g_m \approx 19.2I_{ABC}$  at 25°C. Note that the attenuation of  $V_O$  by  $R$  and  $R_A$  is necessary to maintain  $V_{IN}$  within the linear range of the LM13700 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13700.

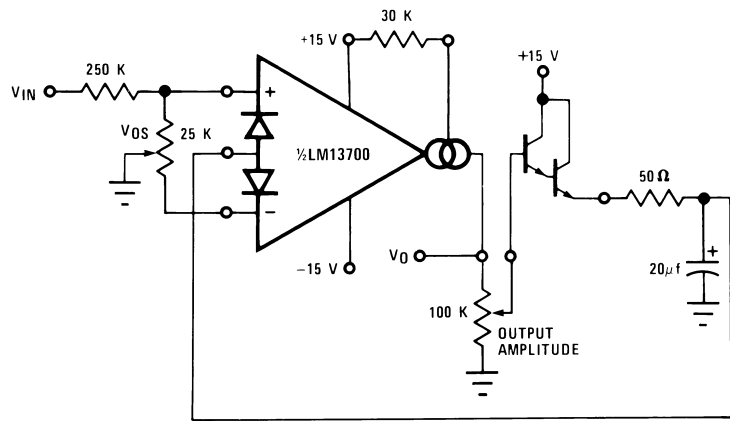
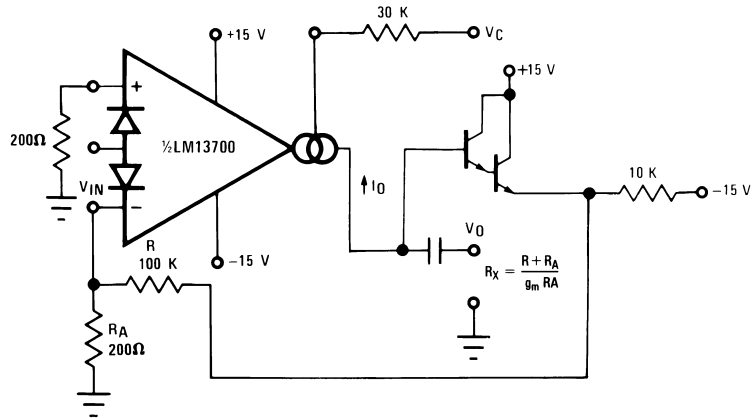


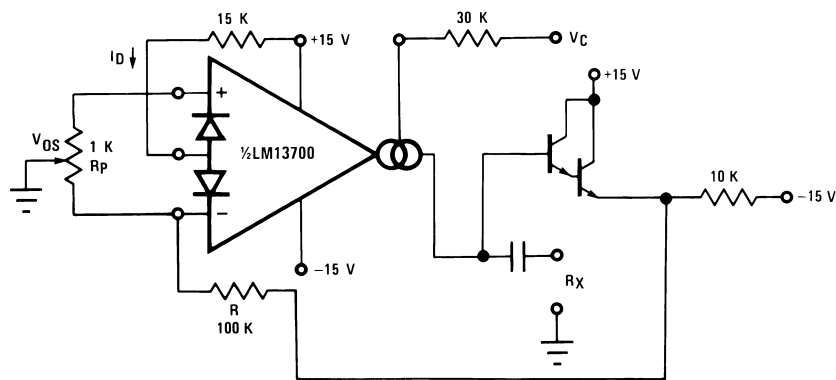
FIGURE 7. AGC Amplifier

## Voltage Controlled Resistors (Continued)



DS007981-15

FIGURE 8. Voltage Controlled Resistor, Single-Ended



DS007981-16

FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

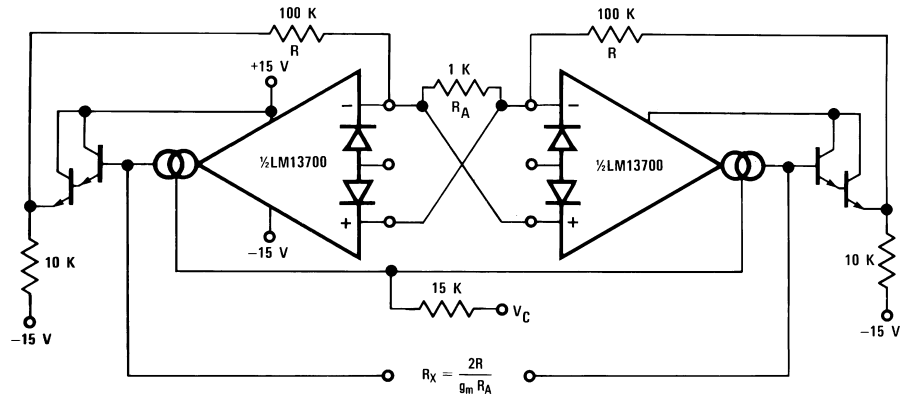
## Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which  $X_C/g_m$  equals the closed-loop gain of  $(R/R_A)$ . At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation, where  $g_m$

is again  $19.2 \times I_{ABC}$  at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

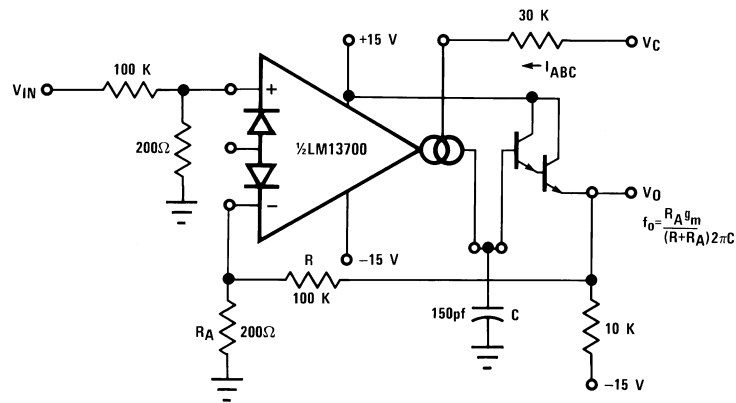
Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent  $g_m$  tracking of the two amplifiers, these filters perform well over several decades of frequency.

## Voltage Controlled Filters (Continued)



DS007981-17

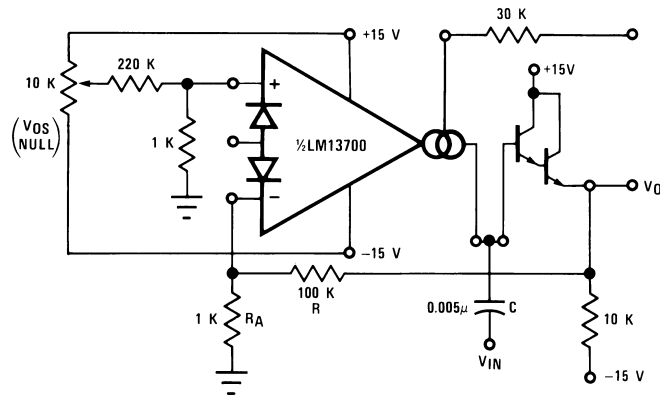
FIGURE 10. Floating Voltage Controlled Resistor



DS007981-18

FIGURE 11. Voltage Controlled Low-Pass Filter

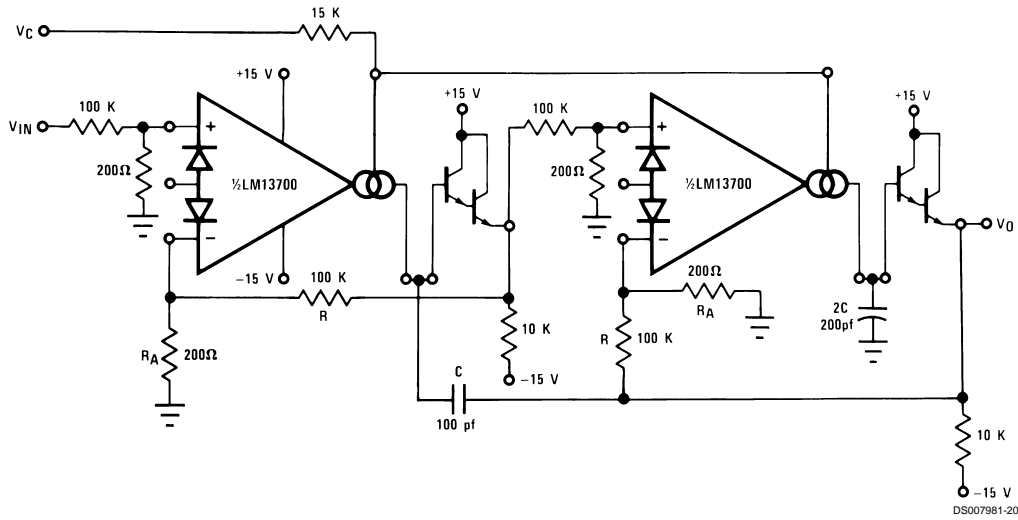
## Voltage Controlled Filters (Continued)



DS007981-19

$$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$$

FIGURE 12. Voltage Controlled Hi-Pass Filter

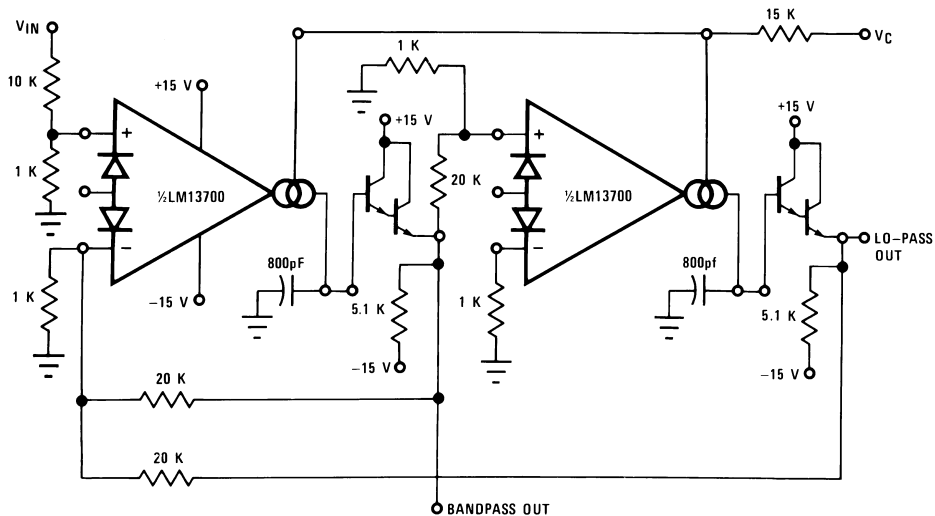


DS007981-20

$$f_o = \frac{R_A g_m}{(R + R_A) 2\pi C}$$

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

## Voltage Controlled Filters (Continued)



DS007981-21

FIGURE 14. Voltage Controlled State Variable Filter

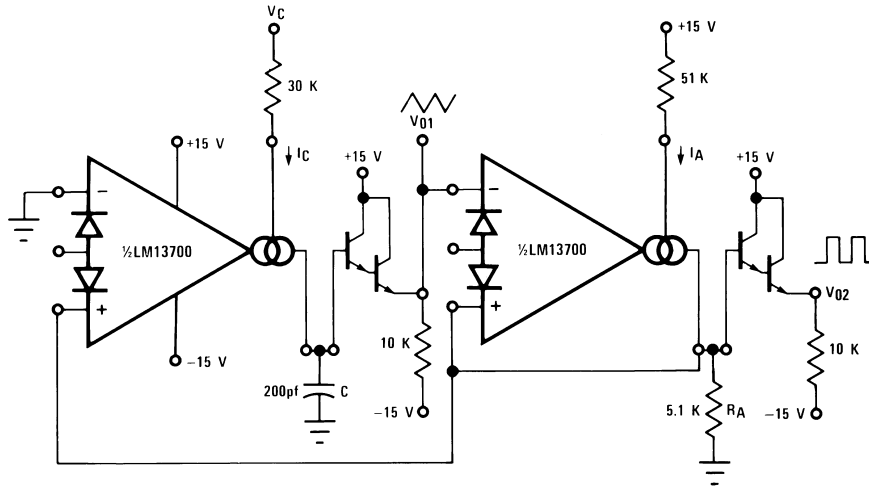
## Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as  $I_C$  is varied from 1 mA to 10 nA. The output amplitudes are set by  $I_A \times R_A$ . Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When  $V_{O2}$  is high,  $I_F$  is added to  $I_C$  to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When  $V_{O2}$  is low,  $I_F$  goes to zero and the capacitor discharge current is set by  $I_C$ .

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is  $360^\circ$  or  $180^\circ$  for the inverter and  $60^\circ$  per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

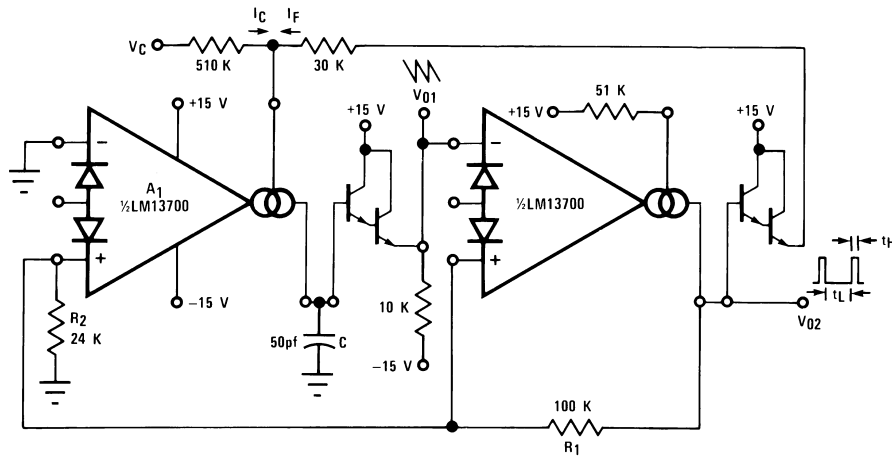
## Voltage Controlled Oscillators (Continued)



DS007981-22

$$f_{\text{OSC}} = \frac{I_C}{4C I_A R_A}$$

FIGURE 15. Triangular/Square-Wave VCO



DS007981-23

$$V_{\text{PK}} = \frac{(V^+ \pm 0.8V) R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{\text{PK}}C}{I_F}$$

$$t_L = \frac{2V_{\text{PK}}C}{I_C}$$

$$f_0 \approx \frac{I_C}{2V_{\text{PK}}C} \text{ for } I_C \ll I_F$$

FIGURE 16. Ramp/Pulse VCO

## Voltage Controlled Oscillators (Continued)

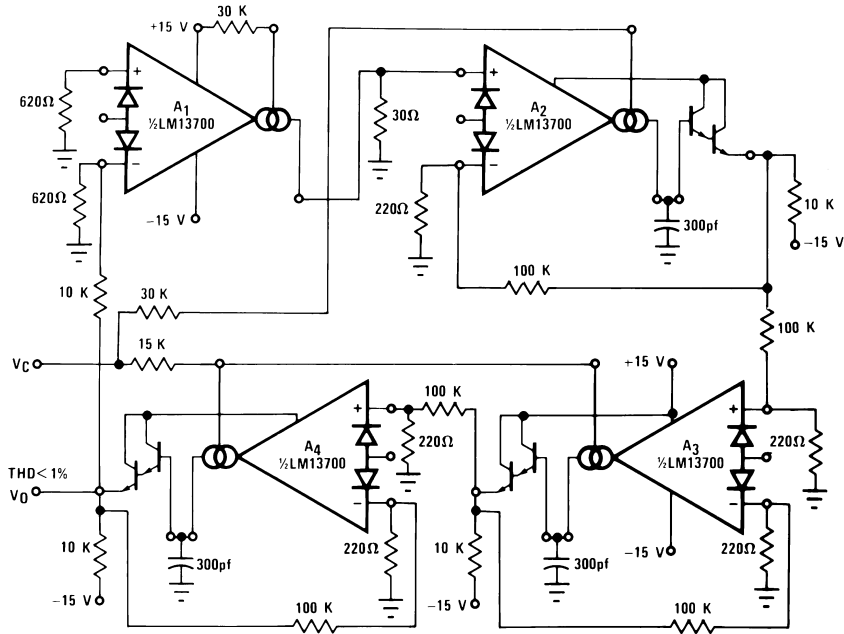


FIGURE 17. Sinusoidal VCO

DS007981-24

## Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through  $R_B$  and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through  $D_1$  when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from  $V_O$ , can perform another function and draw zero stand-by power as well.

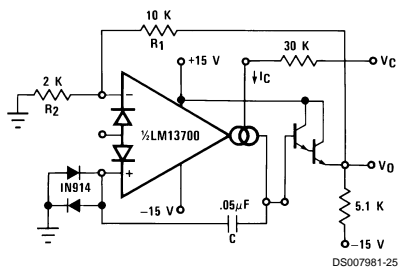
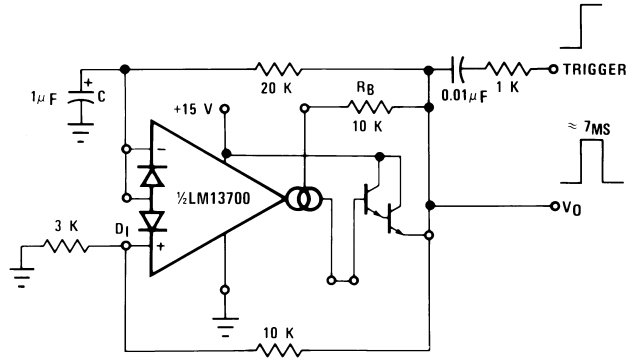


Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

FIGURE 18. Single Amplifier VCO

DS007981-25

## Additional Applications (Continued)

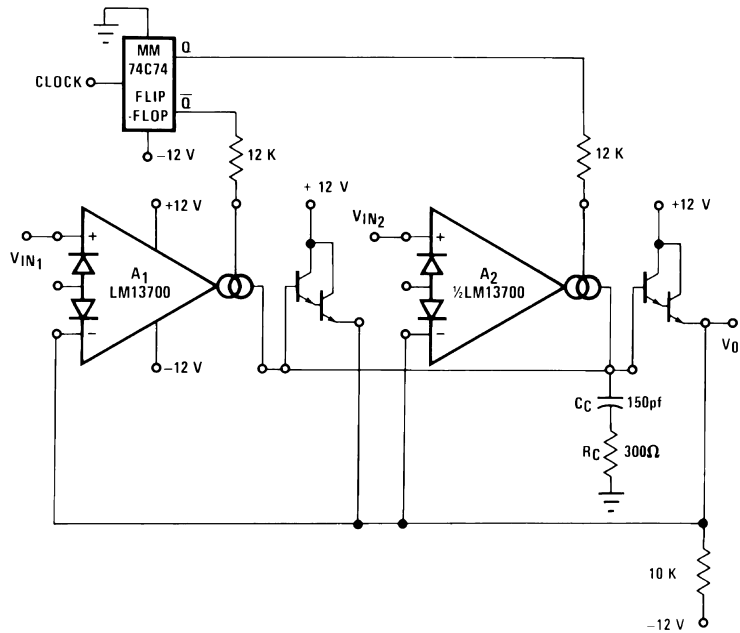


DS007981-26

**FIGURE 19. Zero Stand-By Power Timer**

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds  $V_O$  equal to  $V_{IN1}$  and when A2 is supplied with bias current then it controls  $V_O$ .  $C_C$  and  $R_C$  serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the  $(V_{IN1}-V_{IN2})$  differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a  $\pm 5\%$  hold-in range and an input sensitivity of about 300 mV.

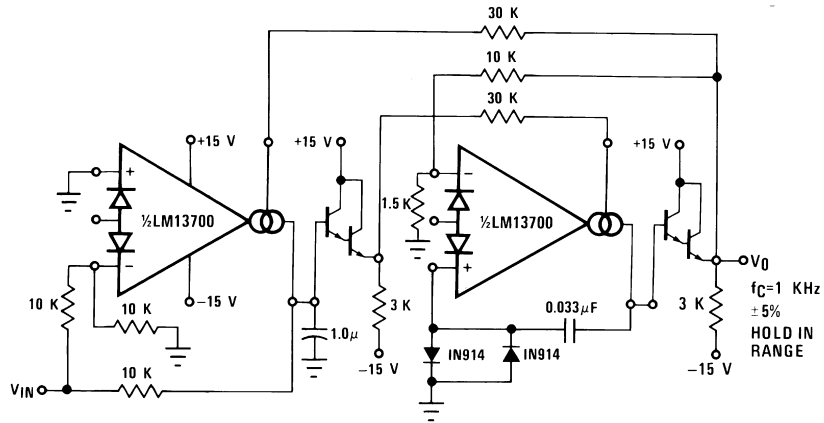


DS007981-27

**FIGURE 20. Multiplexer**



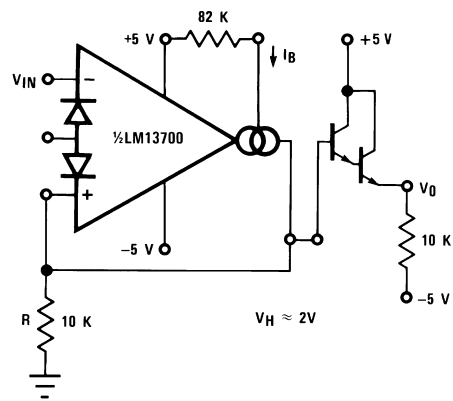
## Additional Applications (Continued)



DS007981-28

**FIGURE 21. Phase Lock Loop**

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus  $V_H = 2 \times R \times I_B$ . Varying  $I_B$  will produce a Schmitt Trigger with variable hysteresis.



DS007981-29

**FIGURE 22. Schmitt Trigger**

## Additional Applications (Continued)

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to  $(V_H - V_L) C_t$  is sourced into  $C_t$  and  $R_t$ . This once per cycle charge is then balanced by the current of  $V_O/R_t$ . The maximum  $F_{IN}$  is limited by the amount of time required to charge  $C_t$  from  $V_L$  to  $V_H$  with a current of  $I_B$ , where  $V_L$  and  $V_H$  represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for  $C_t$  when A1 switches low.

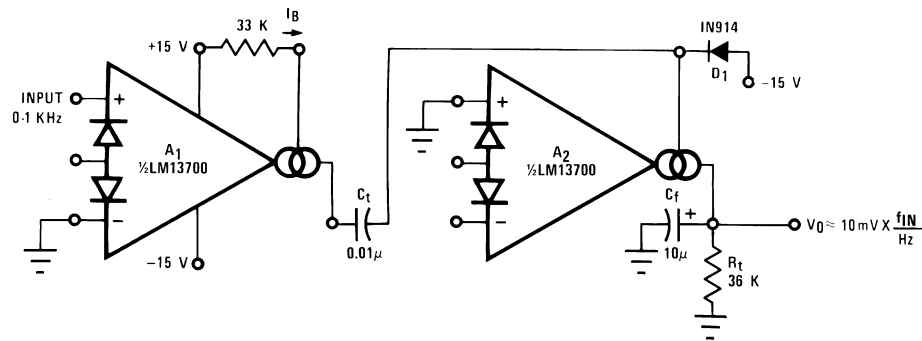


FIGURE 23. Tachometer

DS007981-30

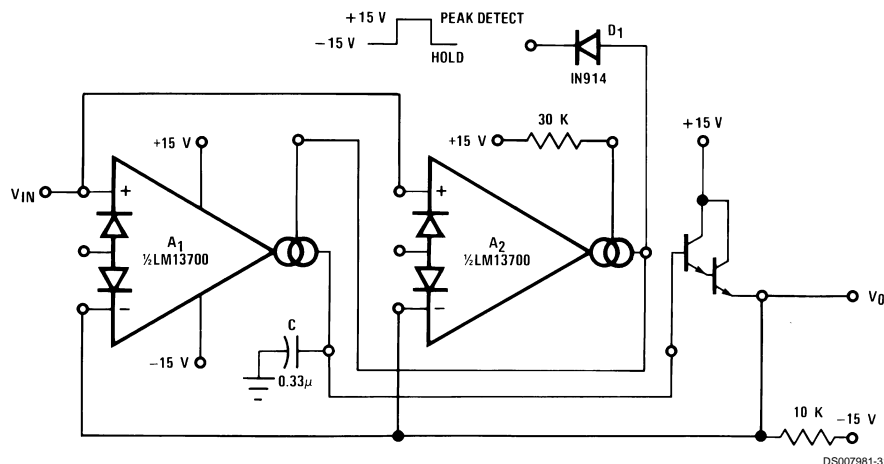


FIGURE 24. Peak Detector and Hold Circuit

DS007981-31

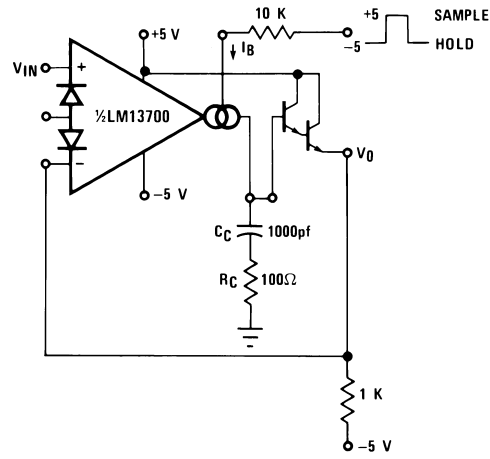
The Ramp-and-Hold of Figure 26 sources  $I_B$  into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to

The Peak Detector of Figure 24 uses A2 to turn on A1 whenever  $V_{IN}$  becomes more positive than  $V_O$ . A1 then charges storage capacitor C to hold  $V_O$  equal to  $V_{IN PK}$ . Pulling the output of A2 low through D1 serves to turn off A1 so that  $V_O$  remains constant.

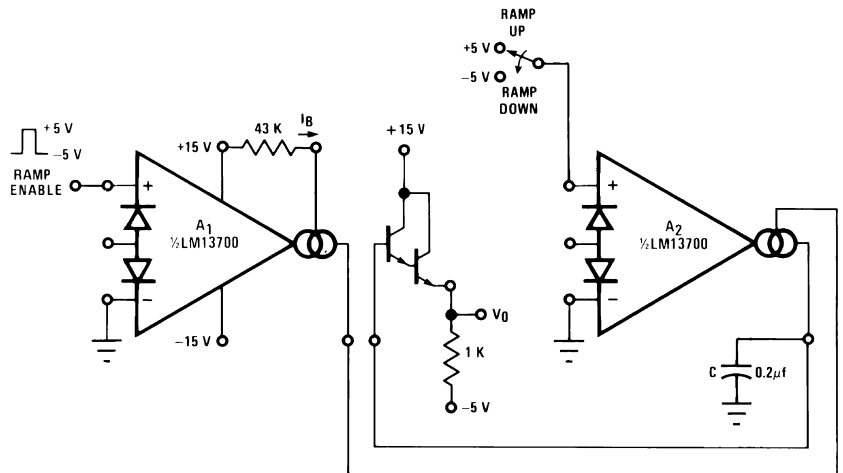
the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that  $V_O$  reads directly in RMS volts.

**Additional Applications** (Continued)



DS007981-32

**FIGURE 25. Sample-and-Hold Circuit**



DS007981-33

**FIGURE 26. Ramp and Hold**

## Additional Applications (Continued)

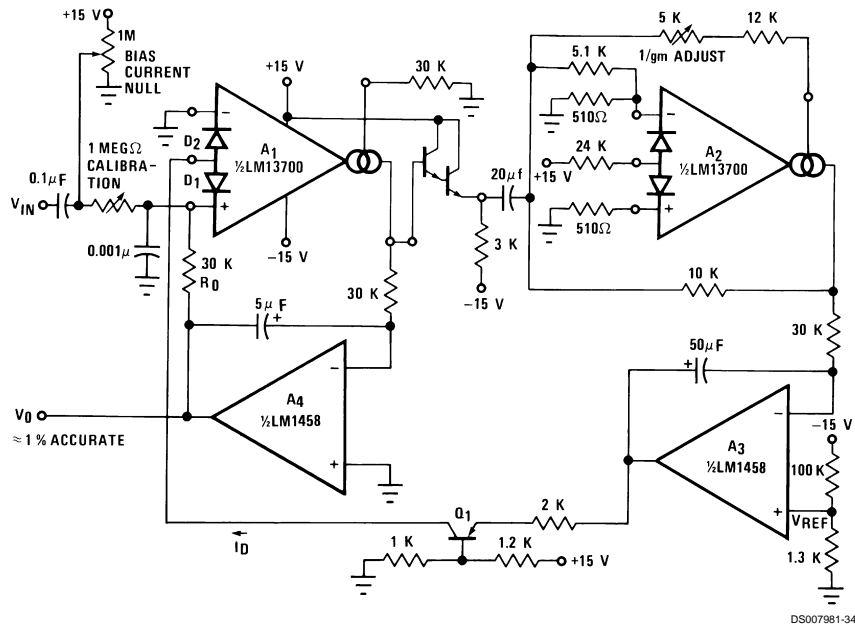


FIGURE 27. True RMS Converter

The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 29.

For generating  $I_{ABC}$  over a range of 4 to 6 decades of current, the system of Figure 30 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to  $I_3 = -V_C/R_C$ .

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From Equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2kTI_3}{qI_2} = \frac{-2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2) V_{IN1}}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B1} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for  $I_{ABC}$  yields:

$$I_{ABC} = I_1 \exp \frac{2(R_1 + R_2) V_C}{R_1 I_2 R_C}$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

## Additional Applications (Continued)

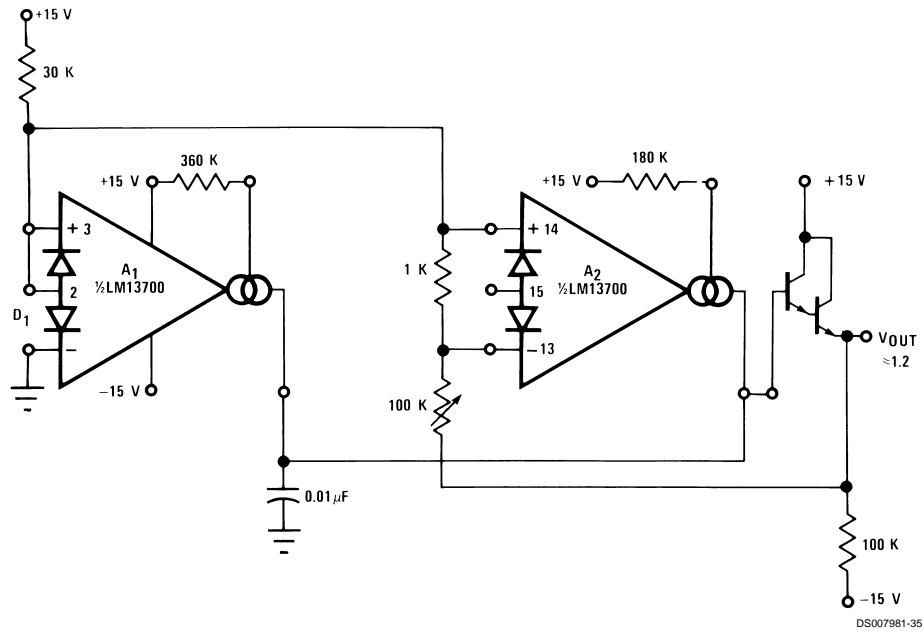


FIGURE 28. Delta VBE Reference

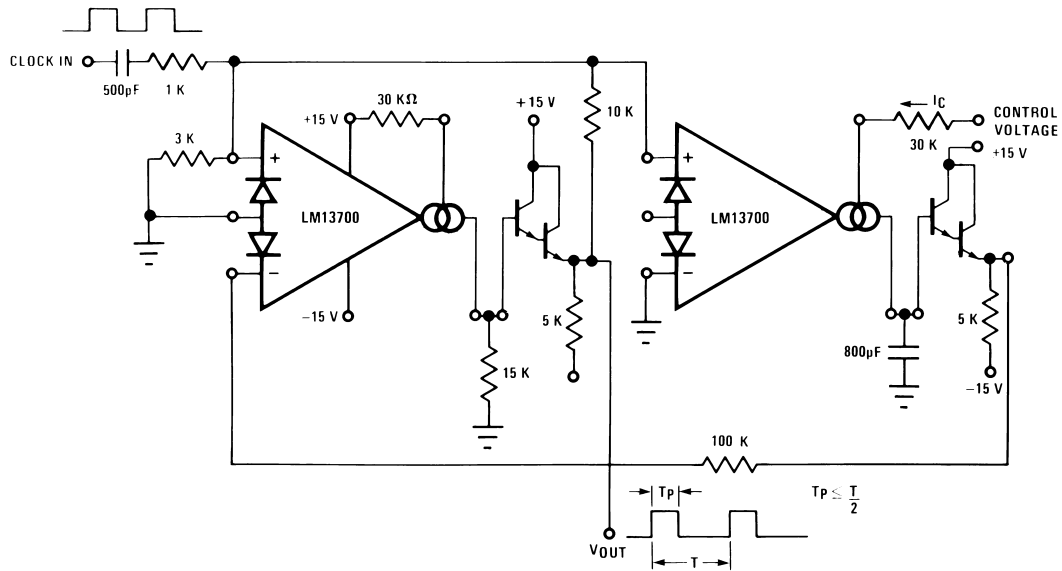
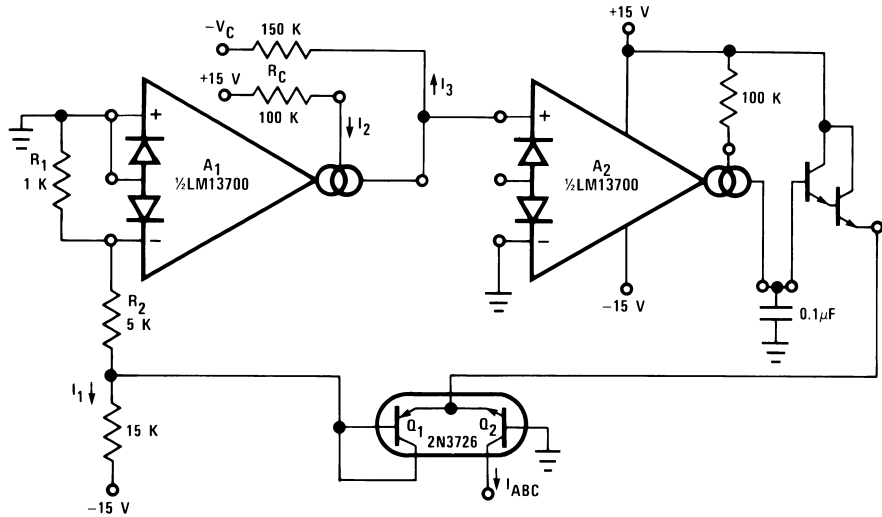


FIGURE 29. Pulse Width Modulator

**Additional Applications** (Continued)

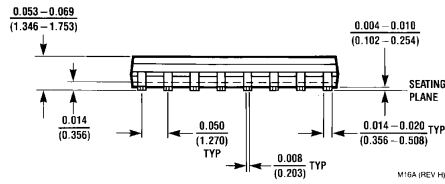
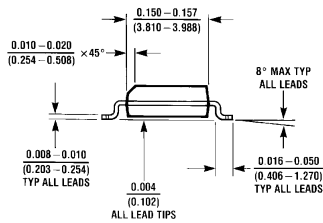
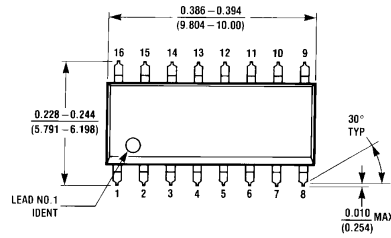


DS007981-37

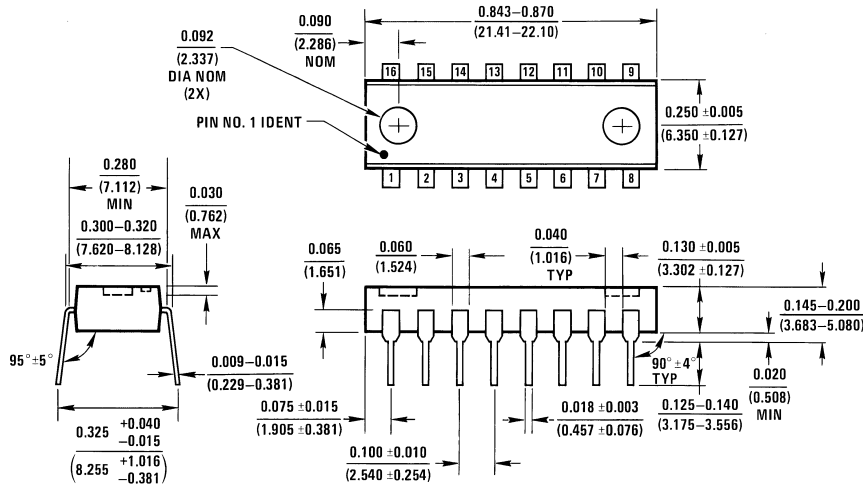
$$I_{ABC} = I_1 \exp \frac{-C I_3}{I_2}$$

**FIGURE 30. Logarithmic Current Source**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**S.O. Package (M)**  
**Order Number LM13700M**  
**NS Package Number M16A**



**Molded Dual-In-Line Package (N)**  
**Order Number LM13700N or LM13700AN**  
**NS Package Number N16A**

## Notes

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

[www.national.com](http://www.national.com)

**National Semiconductor Europe**

Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**

Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**

Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507