

TOSHIBA PHOTOCOUPLER GaAs IRED & PHOTO IC

# TLP582

MOS FET GATE DRIVER

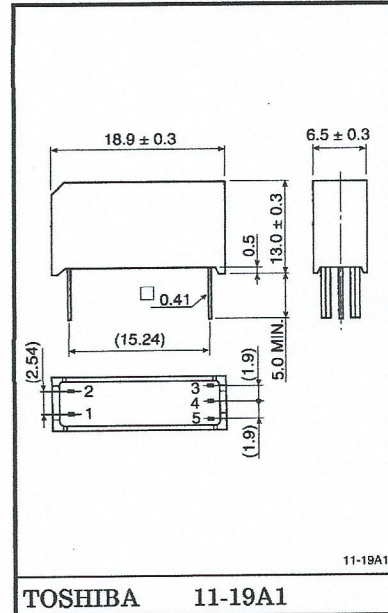
TRANSISTOR INVERTER

The TOSHIBA TLP582 consists of a GaAs light emitting diode and integrated high gain, high speed photodetector.

The detector has a totem pole output circuit that provides source drive and sink drive, and built-in Schmitt trigger.

A fiber is used for light-coupling between LED and detector, and for sufficient separation between input side and output side.

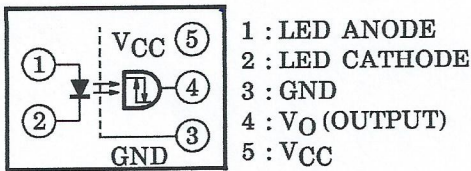
Unit in mm



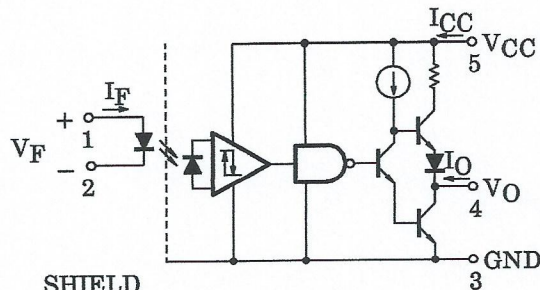
Weight : 1.55g

- Input Current :  $I_F = 5\text{mA (MAX.)}$
- Power Supply Voltage :  $V_{CC} = 4.5 \sim 20\text{V}$
- Switching Speed :  $t_{pHL}, t_{pLH} = 400\text{ns (MAX.)}$
- Common Mode Transient Immunity :  $\pm 5000\text{V} / \mu\text{s (MIN.)}$
- Guaranteed Performance Over Temperature :  $-25 \sim 85^\circ\text{C}$
- Isolation Voltage :  $5000V_{\text{RMS (MIN.)}}$
- UL Recognized : UL1577, File No. E67349

PIN CONFIGURATION (TOP VIEW)



SCHEMATIC



SHIELD

A  $0.1\mu\text{F}$  bypass capacitor must be connected between pins 3 and 5.

TRUTH TABLE (Positive Logic)

INPUT	OUTPUT
H	L
L	H

961001EBC2

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## MAXIMUM RATINGS

(No Derating Required up to 85°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	$I_F$	25	mA
	Peak Transient Forward Current (Note 1)	$I_{FPT}$	1	A
	Reverse Voltage	$V_R$	5	V
DETECTOR	Output Current	$I_O$	40 / -25	mA
	Peak Output Current (Note 2)	$I_{OP}$	80 / -50	mA
	Output Voltage	$V_O$	-0.5~20	V
	Supply Voltage	$V_{CC}$	-0.5~20	V
	Output Power Dissipation (Note 3)	$P_O$	100	mW
	Total Package Power Dissipation (Note 4)	$P_T$	200	mW
	Operating Temperature Range	$T_{opr}$	-40~85	°C
Storage Temperature Range	$T_{stg}$	-40~100	°C	
Lead Solder Temperature (10s)	$T_{sol}$	260	°C	
Isolation Voltage (AC, 1min., R.H. ≤ 60%, $T_a = 25^\circ\text{C}$ ) (Note 5)	$BV_S$	5000	$V_{rms}$	

(Note 1) Pulse Width  $\leq 1\mu\text{s}$ , 300pps.(Note 2) Pulse Width  $\leq 5\mu\text{s}$ , Duty Ratio  $\leq 0.025$ .

(Note 3) Derate 1.8mW/°C above 70°C ambient temperature.

(Note 4) Derate 3.6mW/°C above 70°C ambient temperature.

(Note 5) Device considered a two terminal device : pins 1, 2 shorted together, and pins 3, 4 and 5 shorted together.

## RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, ON	$I_F(\text{ON})$	7	8	20	mA
Input Voltage, OFF	$V_F(\text{OFF})$	0	—	0.8	V
Supply Voltage	$V_{CC}$	4.5	—	20	V
Operating Temperature	$T_{opr}$	-25	—	85	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified,  $T_a = -25 \sim 85^\circ\text{C}$ ,  $V_{CC} = 4.5 \sim 20\text{V}$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT	
Input Forward Voltage	$V_F$	$I_F = 5\text{mA}$ , $T_a = 25^\circ\text{C}$	—	1.35	1.85	V	
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_a$	$I_F = 5\text{mA}$	—	-2	—	mV/°C	
Input Reverse Current	$I_R$	$V_R = 3\text{V}$ , $T_a = 25^\circ\text{C}$	—	—	100	$\mu\text{A}$	
Input Capacitance	$C_T$	$V_F = 0$ , $f = 1\text{MHz}$ , $T_a = 25^\circ\text{C}$	—	170	—	pF	
Output Leakage Current ( $V_O > V_{CC}$ )	$I_{OHH}$	$V_F = 0\text{V}$ $V_{CC} = 4.5\text{V}$	$V_O = 5.5\text{V}$	—	—	100	$\mu\text{A}$
			$V_O = 20\text{V}$	—	0.01	500	
Logic Low Output Voltage	$V_{OL}$	$I_{OL} = 6.4\text{mA}$ , $I_F = 5\text{mA}$	—	0.4	0.5	V	
Logic High Output Voltage	$V_{OH}$	$I_{OH} = -2.6\text{mA}$ , $V_F = 0.8\text{V}$	2.4	3.3	—	V	
Logic Low Supply Current	$I_{CCL}$	$I_F = 7.5\text{mA}$	$V_{CC} = 5.5\text{V}$	—	4.0	6.0	mA
			$V_{CC} = 20\text{V}$	—	4.6	7.5	
Logic High Supply Current	$I_{CCH}$	$V_F = 0\text{V}$	$V_{CC} = 5.5\text{V}$	—	4.2	6.0	mA
			$V_{CC} = 20\text{V}$	—	4.7	7.5	
Logic Low Short Circuit Output Current (Note 6)	$I_{OSL}$	$I_F = 7.5\text{mA}$	$V_O = V_{CC} = 5.5\text{V}$	25	55	—	mA
			$V_O = V_{CC} = 20\text{V}$	40	80	—	
Logic High Short Circuit Output Current (Note 6)	$I_{OSH}$	$V_F = 0\text{V}$ $V_O = \text{GND}$	$V_{CC} = 5.5\text{V}$	-10	-25	—	mA
			$V_{CC} = 20\text{V}$	-25	-60	—	
Input Current Logic Low Output	$I_{FL}$	$I_O = 6.4\text{mA}$ , $V_O < 0.4\text{V}$	—	—	5	mA	
Input Voltage Logic High Output	$V_{FH}$	$I_O = -2.6\text{mA}$ , $V_O > 2.4\text{V}$	0.8	—	—	V	
Input Current Hysteresis	$I_{HYS}$	$V_{CC} = 5\text{V}$	—	0.05	—	mA	
Resistance (Input-Output)	$R_S$	$V_S = 500\text{V}$ , R.H. $\leq 60\%$ $T_a = 25^\circ\text{C}$ (Note 5)	$5 \times 10^{10}$	$10^{14}$	—	$\Omega$	
Capacitance (Input-Output)	$C_S$	$V_S = 0$ , $f = 1\text{MHz}$ , $T_a = 25^\circ\text{C}$ (Note 5)	—	0.15	0.3	pF	

\* All typical values are at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_F (\text{ON}) = 7.5\text{mA}$  unless otherwise specified.

SWITCHING CHARACTERISTICS (Unless Otherwise specified,  $V_{CC} = 4.5 \sim 20V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.*	MAX.	UNIT
Propagation Delay Time to Logic High Output (Note 7)	$t_{pLH}$	1	$I_F = 7.5 \rightarrow 0mA$	—	250	400	ns
Propagation Delay Time to Logic Low Output (Note 7)	$t_{pHL}$		$I_F = 0 \rightarrow 7.5mA$	—	270	400	ns
Output Rise Time (10-90%)	$t_r$		$I_F = 7.5 \rightarrow 0mA$ , $V_{CC} = 5V$	—	35	75	ns
Output Fall Time (90-10%)	$t_f$		$I_F = 0 \rightarrow 7.5mA$ , $V_{CC} = 5V$	—	20	75	ns
Common Mode Transient Immunity at Logic High Output (Note 8)	$C_{MH}$	2	$I_F = 0mA$ , $V_{CM} = 400V$ $V_O (Min.) = 2V$	5	10	—	$kV / \mu s$
Common Mode Transient Immunity at Logic Low Output (Note 8)	$C_{ML}$		$I_F = 7.5mA$ , $V_{CM} = 400V$ $V_O (Max.) = 0.8V$	-5	-10	—	$kV / \mu s$

\* All typical values are at  $T_a = 25^\circ C$ ,  $V_{CC} = 5V$

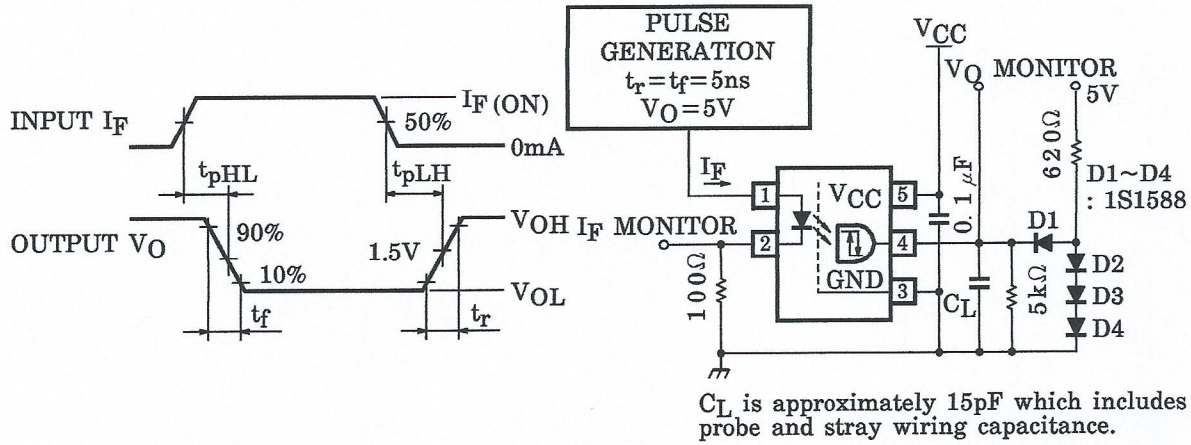
(Note 6) Duration of output short circuit time should not exceed 10ms.

(Note 7) The  $t_{pLH}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5V point on the leading edge of the output pulse.  
The  $t_{pHL}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

(Note 8)  $C_{ML}$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 0.8V$ ).  
 $C_{MH}$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 2.0V$ ).

(Note 9) A ceramic capacitor ( $0.1\mu F$ ) should be connected from pin 3 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

TEST CIRCUIT 1 :  $t_{pHL}$ ,  $t_{pLH}$ ,  $t_r$  and  $t_f$



TEST CIRCUIT 2 : Common Mode Transient Immunity

