

ULN2803A Darlington Transistor Arrays

Check for Samples: [ULN2803A](#)

FEATURES

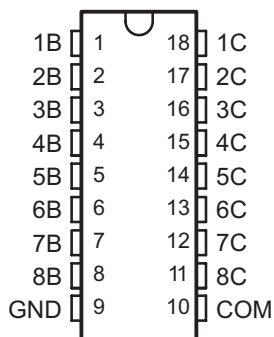
- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs: 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**
- **Compatible with ULN2800A Series**

DESCRIPTION

The ULN2803A device is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A device has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

**DW OR N PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ULN2803A

SLRS049F – FEBRUARY 1997 – REVISED JANUARY 2014

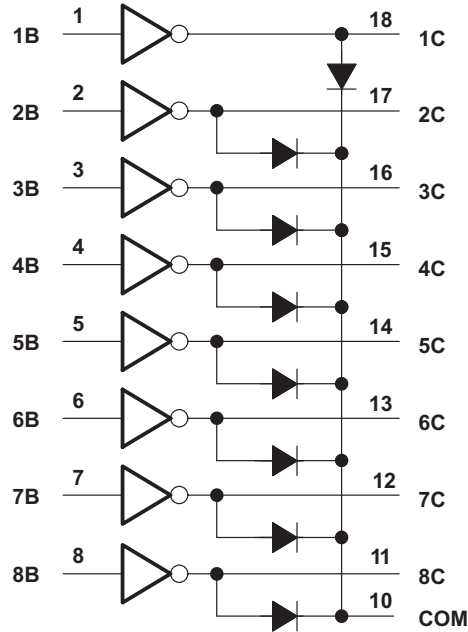
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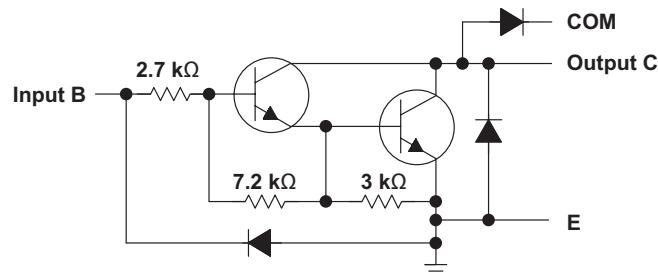
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Logic Diagram



Schematic (Each Darlington Pair)



Absolute Maximum Ratings⁽¹⁾

at 25°C free-air temperature (unless otherwise noted)

		VALUE	UNIT	
	Collector-emitter voltage	50	V	
	Input voltage ⁽²⁾	30	V	
	Peak collector current	500	mA	
	Output clamp current	500	mA	
	Total substrate-terminal current	–2.5	A	
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package	73.14	°C/W
		DW package	62.66	
T_J	Operating virtual junction temperature	150	°C	
T_{stg}	Storage temperature range	–65 to 150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.
- (3) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics

 at $T_A = 25^\circ\text{C}$ free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ULN2002A			UNIT		
		MIN	TYP	MAX			
I_{CEX}	Collector cutoff current	$V_{CE} = 50\text{ V}$, see Figure 1		$I_I = 0$	50	μA	
$I_{I(\text{off})}$	Off-state input current	$V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$		$I_C = 500\ \mu\text{A}$, see Figure 2	50	65	μA
$I_{I(\text{on})}$	Input current	$V_I = 3.85\text{ V}$,		See Figure 3	0.93	1.35	mA
$V_{I(\text{on})}$	On-state input voltage	$V_{CE} = 2\text{ V}$, see Figure 4		$I_C = 200\text{ mA}$	2.4		V
				$I_C = 250\text{ mA}$	2.7		
				$I_C = 300\text{ mA}$	3		
$V_{CE(\text{sat})}$	Collector-emitter saturation voltage	$I_I = 250\ \mu\text{A}$, see Figure 5		$I_C = 100\text{ mA}$	0.9	1.1	V
		$I_I = 350\ \mu\text{A}$, see Figure 5		$I_C = 200\text{ mA}$	1	1.3	
		$I_I = 500\ \mu\text{A}$, see Figure 5		$I_C = 350\text{ mA}$	1.3	1.6	
I_R	Clamp diode reverse current	$V_R = 50\text{ V}$,		see Figure 6	50		μA
V_F	Clamp diode forward voltage	$I_F = 350\text{ mA}$		see Figure 7	1.7	2	V
C_i	Input capacitance	$V_I = 0$,		$f = 1\text{ MHz}$	15	25	pF

Switching Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	Propagation delay time, low- to high-level output	$V_S = 50\text{ V}$, $C_L = 15\text{ pF}$, $R_L = 163\ \Omega$, See Figure 8			ns	
t_{PHL}	Propagation delay time, high- to low-level output	20				
V_{OH}	High-level output voltage after switching	$V_S = 50\text{ V}$, $I_O = 300\text{ mA}$, See Figure 9			$V_S - 20$	mV

Parameter Measurement Information

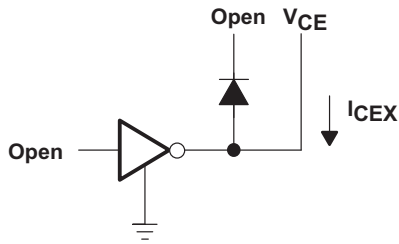


Figure 1. I_{CEX} Test Circuit

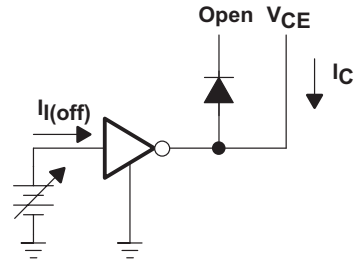


Figure 2. $I_{I(off)}$ Test Circuit

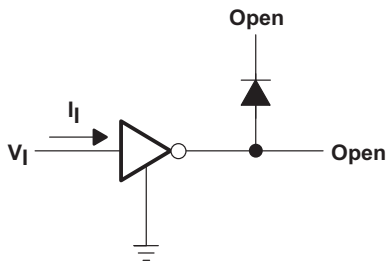


Figure 3. $I_{I(on)}$ Test Circuit

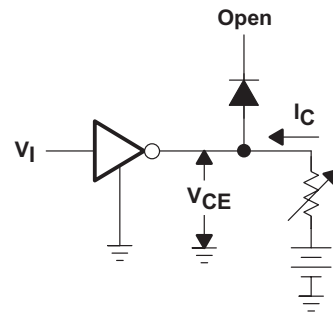


Figure 4. $V_{I(on)}$ Test Circuit

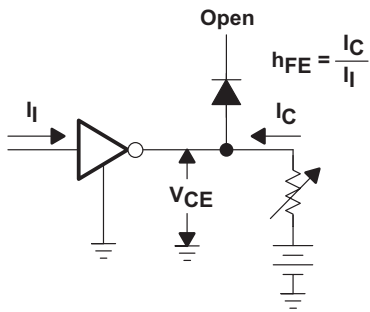


Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

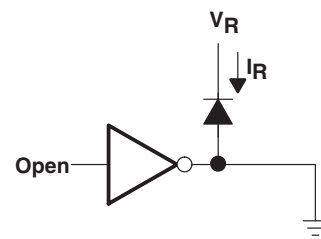


Figure 6. I_R Test Circuit

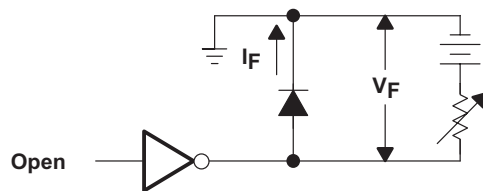
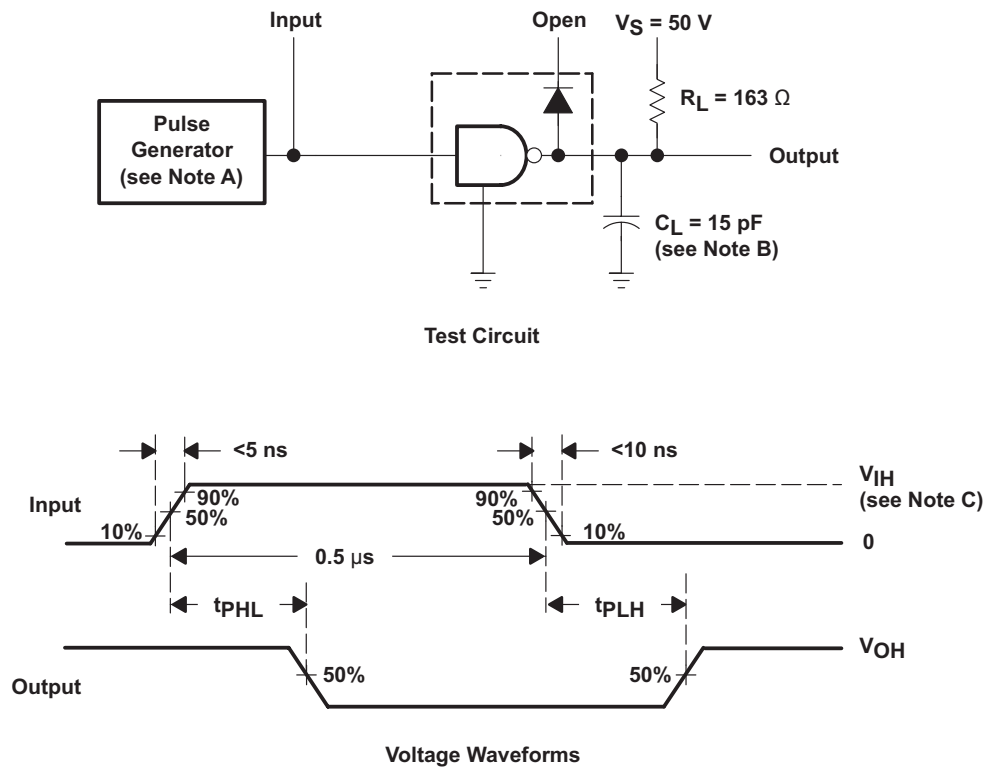


Figure 7. V_F Test Circuit

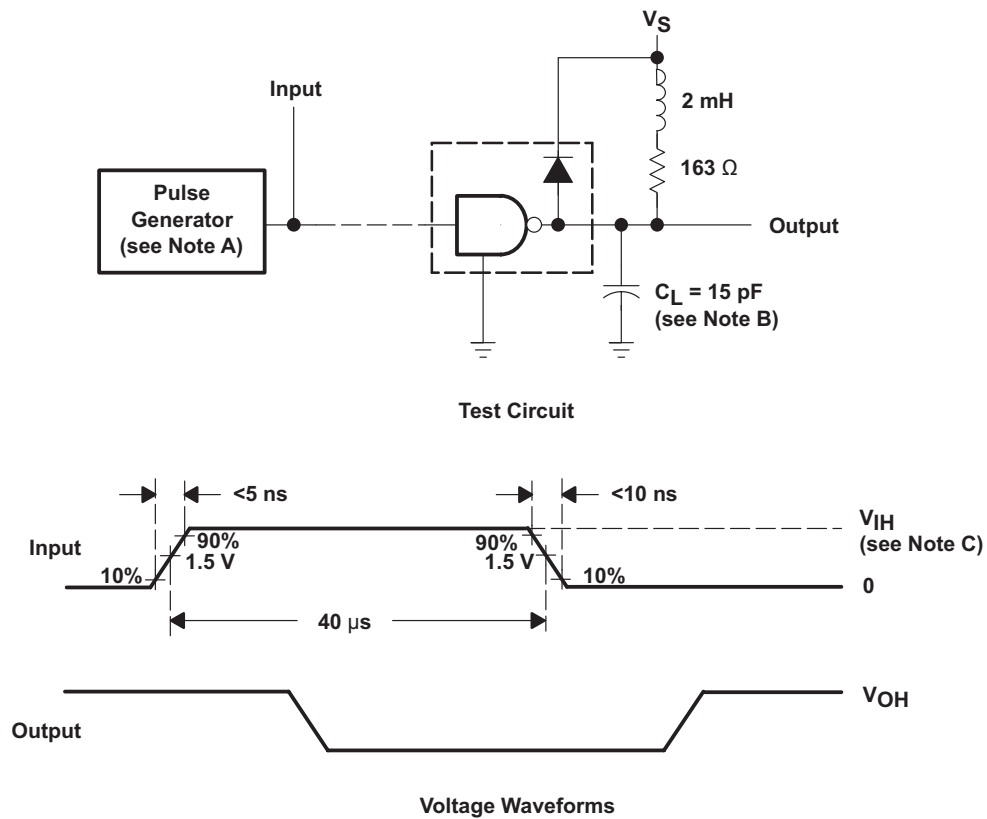
Parameter Measurement Information (continued)



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. $V_{IH} = 3 \text{ V}$

Figure 8. Propagation Delay-Times

Parameter Measurement Information (continued)



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. $V_{IH} = 3$ V

Figure 9. Latch-Up Test

REVISION HISTORY

Changes from Revision E (July 2006) to Revision F	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Deleted Ordering Information table.	1
• Added ESD warning.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2803ADW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803ADWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ULN2803A	Samples
ULN2803AN	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	ULN2803AN	Samples
ULN2803ANE4	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	ULN2803AN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803ADWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

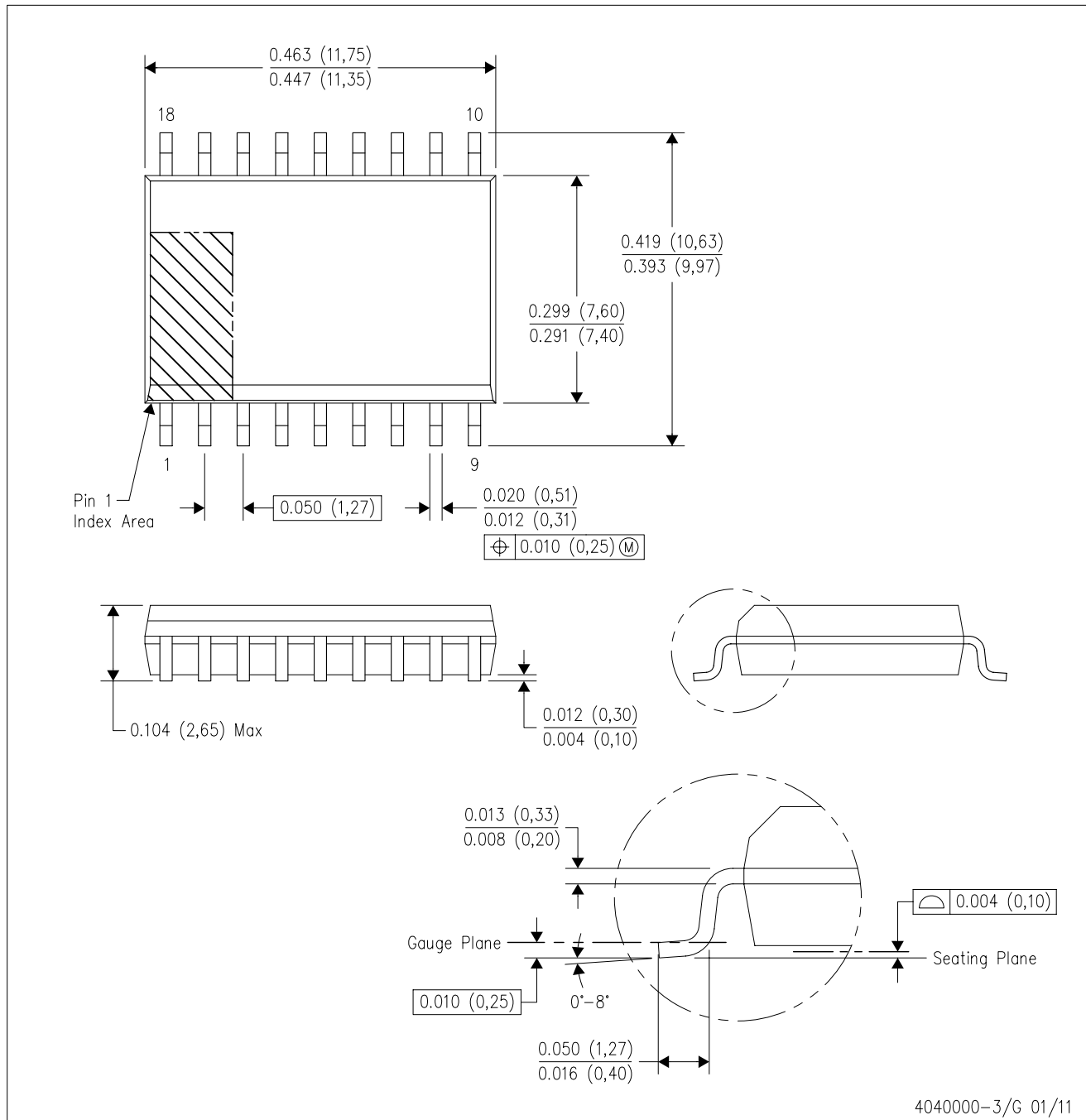


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2803ADWR	SOIC	DW	18	2000	370.0	355.0	55.0

DW (R-PDSO-G18)

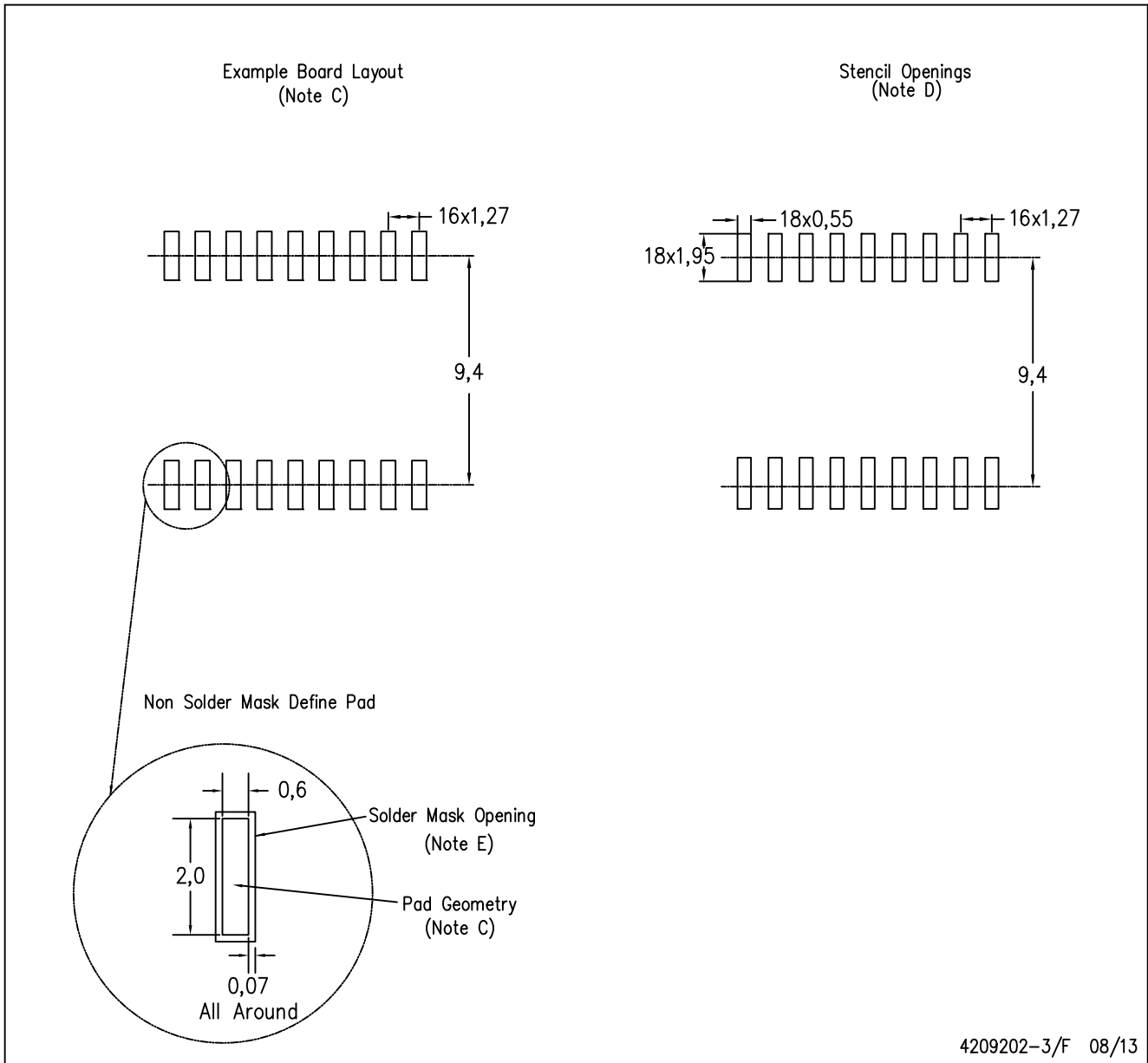
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AB.

DW (R-PDSO-G18)

PLASTIC SMALL OUTLINE



4209202-3/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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