TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

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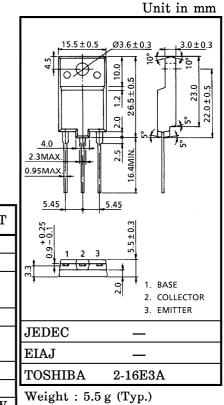
COLOR TV HORIZONTAL OUTPUT APPLICATIONS

COLOR TV SWITCHING REGULATOR APPLICATIONS

- High Voltage  $: V_{CES} = 1500 V$
- High Speed :  $t_f = 0.7 \ \mu s$  (Max.)
- Low Saturation Voltage : V<sub>CE (sat)</sub> = 5 V (Max.)
- Collector Metal (Fin) is Fully Covered with Mold Resin. ((IS) Package)

## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT	
Collector-Base Voltage		VCES	1500	V	
Emitter-Base Voltage		VEBO	5	V	
Collector Current	DC	IC	8	- A	
	Pulse	I <sub>CP</sub>	15		
Base Current		IB	4	Α	
Collector Power Dissipation ( $Tc = 25^{\circ}C$ )		PC	P <sub>C</sub> 50		
Junction Temperature		T <sub>j</sub> 150		°C	
Storage Temperature Range		$T_{stg} = -55 \sim 150$		°C	
Thermal Resistance		R <sub>th (j-c)</sub>	2.5	°C/W	



## ELECTRICAL CHARACTERISTICS (Ta = 25°C)

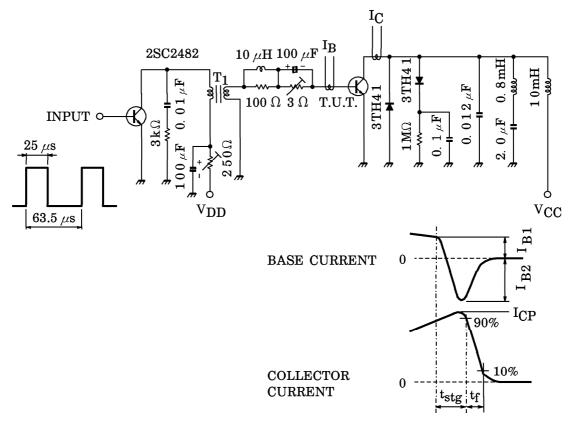
	OVMDOT	TEST CONDITION	MINT	<b>TIVD</b>	MAY	TINIT
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	ICBO	$V_{CB} = 1500 V, V_{BE} = 0$	_	_	1	mA
Emitter-Base Breakdown	V <sub>EBO</sub>	$I_E = 1 \text{ mA}, I_C = 0$	5			v
Voltage	▼EBO					v
DC Current Gain	h <sub>FE</sub> (1)	$V_{CE} = 5 V, I_{C} = 1 A$	10	_	30	
	h <sub>FE</sub> (2)	$V_{CE} = 5 V, I_{C} = 4.5 A$	4.5	—	9	
Collector-Emitter Saturation	N7 eren in the	$I_{C} = 4.5 \text{ A}, I_{B} = 2 \text{ A}$	_	—	1	v
Voltage	VCE (sat)	$I_{C} = 4.5 \text{ A}, I_{B} = 1 \text{ A}$	_	—	5	
<b>Base-Emitter Saturation</b>	Varia	$I_{C} = 4.5 \text{ A}, I_{B} = 1 \text{ A}$	_	0.9	1.2	v
Voltage	V <sub>BE</sub> (sat)					
Collector-Emitter Sustain	Voru	$L = 40 \text{ mH}, I_{B} = 500 \text{ mA}$	700		_	v
Voltage	VCEX (sus)	$V_{BE} = -1.7 V$				
Transition Frequency	$f_{T}$	$V_{CE} = 10 V, I_{C} = 0.1 A$	_	2	—	MHz
Collector Output Capacitance	Cob	$V_{CB} = 10 V, I_E = 0, f = 1 MHz$	_	95	—	pF
Switching Time Storage Time	t <sub>stg</sub>	$I_{CP} = 4.5 \text{ A}, I_{B1} \text{ (end)} = 1 \text{ A}$	_	8	12	
(Fig.1) Fall Time	tf	$f_{\rm H} = 15.75  \mathrm{kHz}$	_	0.4	0.7	$\mu$ s

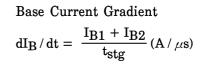
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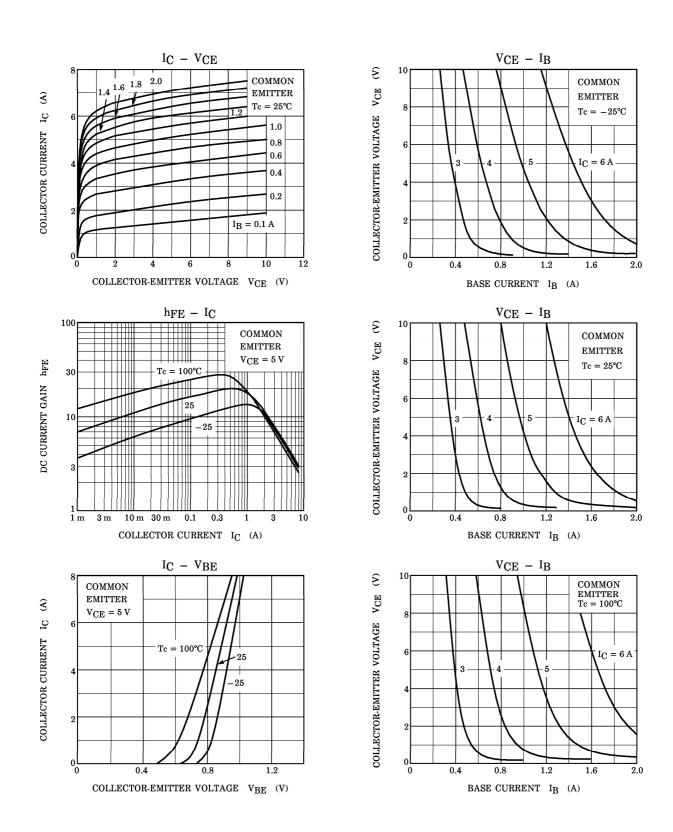
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Fig.1 SWITCHING TIME TEST CIRCUIT





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