

**Silicon PNP Power Transistors**

**2SB863**

**DESCRIPTION**

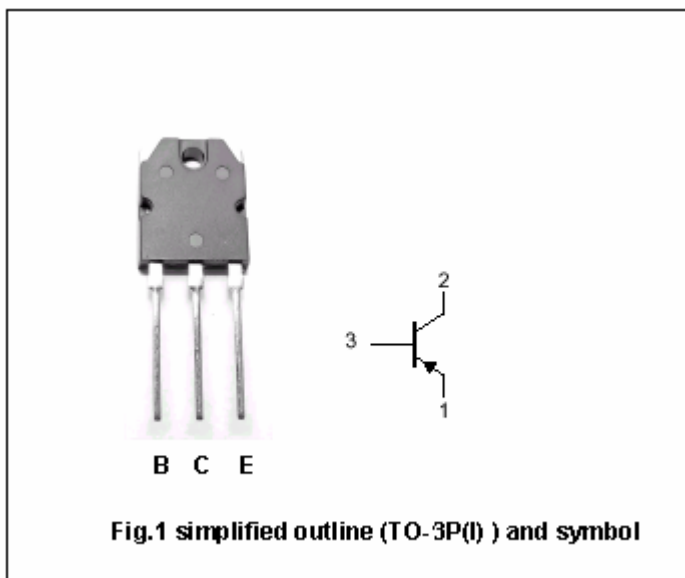
- With TO-3P(I) package
- Complement to type 2SD1148

**APPLICATIONS**

- Power amplifier applications
- Recommend for 70W high fidelity audio frequency amplifier output stage

**PINNING**

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



**Absolute maximum ratings(Ta=25 )**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	-140	V
$V_{CEO}$	Collector-emitter voltage	Open base	-140	V
$V_{EBO}$	Emitter-base voltage	Open collector	-5	V
$I_C$	Collector current		-10	A
$I_B$	Base current		-1	A
$P_C$	Collector power dissipation	$T_C=25$	100	W
$T_j$	Junction temperature		150	
$T_{stg}$	Storage temperature		-55~150	

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =-50mA; I <sub>B</sub> =0	-140			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-5.0A; I <sub>B</sub> =-0.5A		-0.60	-2.0	V
V <sub>BE</sub>	Base-emitter on voltage	I <sub>C</sub> =-5A; V <sub>CE</sub> =-5V		-0.96	-1.5	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-140V; I <sub>E</sub> =0			-5.0	μA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-5V; I <sub>C</sub> =0			-5.0	μA
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =-1A; V <sub>CE</sub> =-5V	55		160	
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =-5A; V <sub>CE</sub> =-5V	25			
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =-1A; V <sub>CE</sub> =-10V		15		MHz
C <sub>OB</sub>	Collector output capacitance	I <sub>C</sub> =0; f=1MHz; V <sub>CB</sub> =-10V		400		pF

◆ h<sub>FE-1</sub> Classifications

R	O
55-110	80-160

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PACKAGE OUTLINE

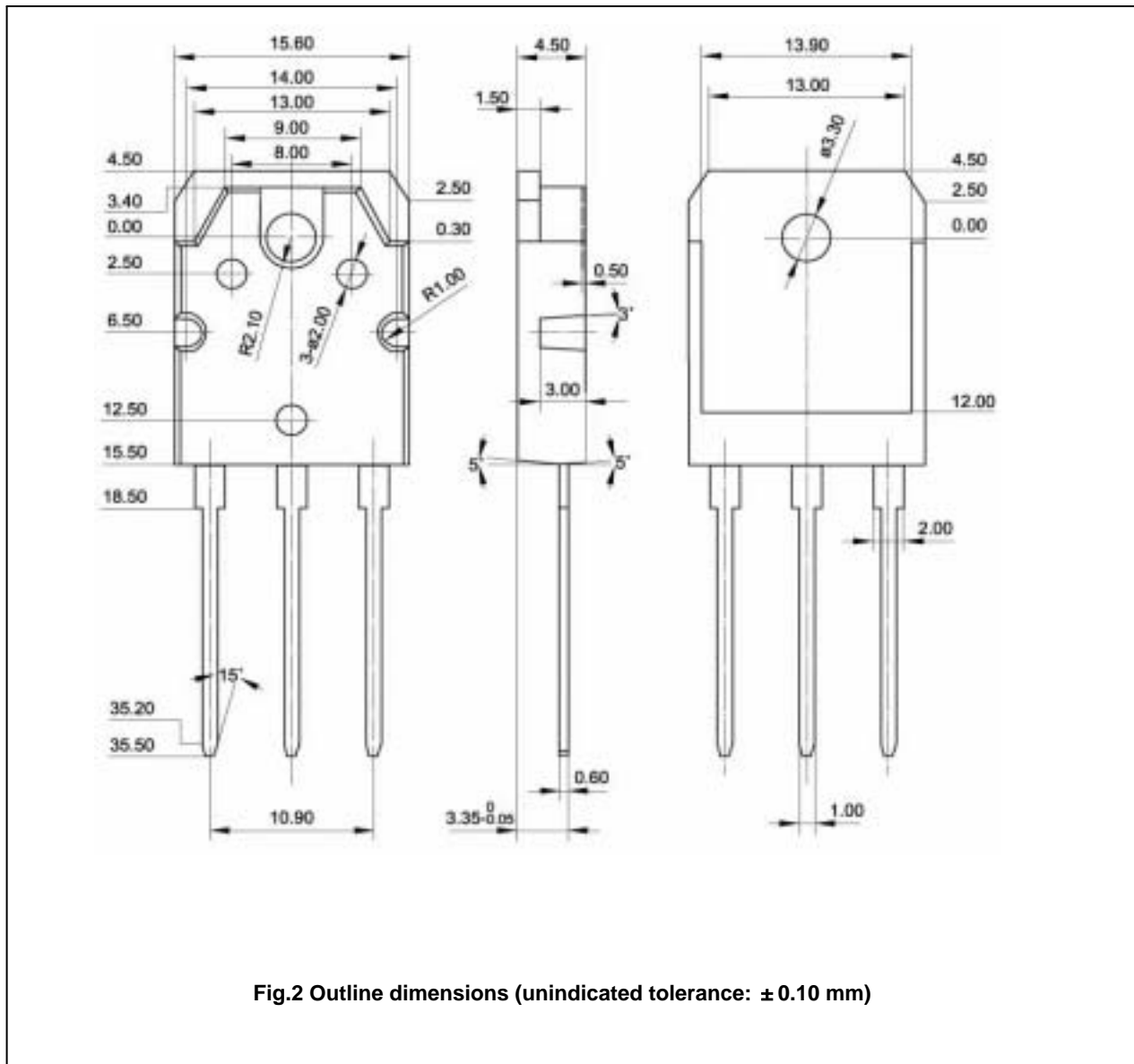


Fig.2 Outline dimensions (unindicated tolerance: ±0.10 mm)

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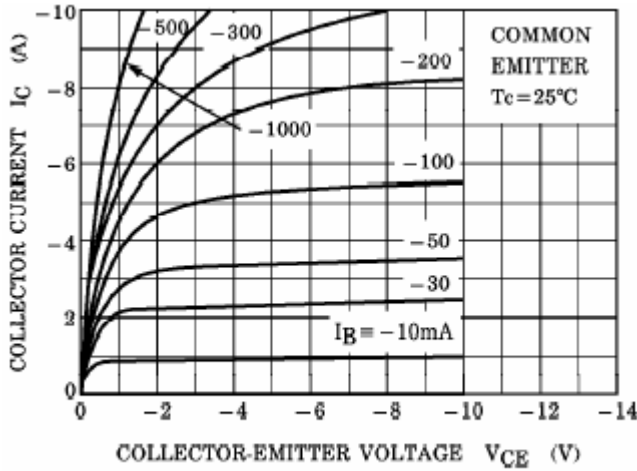


Fig.3 Static Characteristic

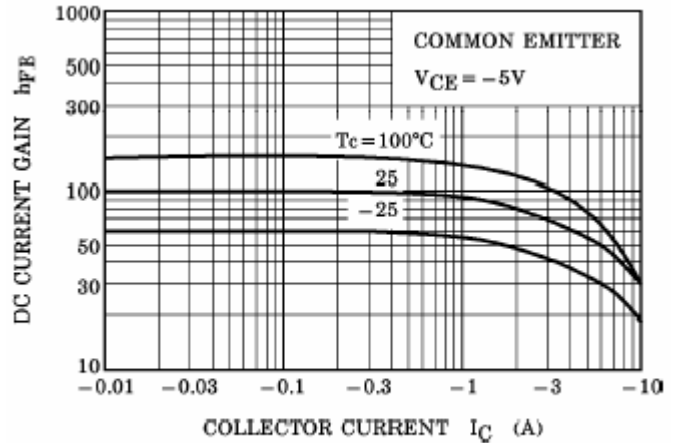


Fig.4 DC current Gain

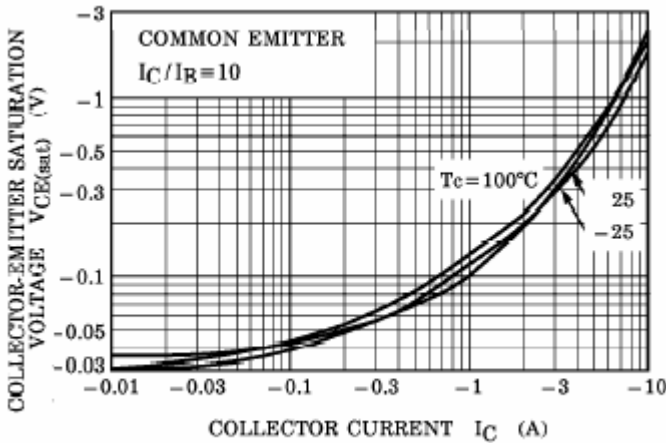


Fig.5 Collector-Emitter Saturation Voltage

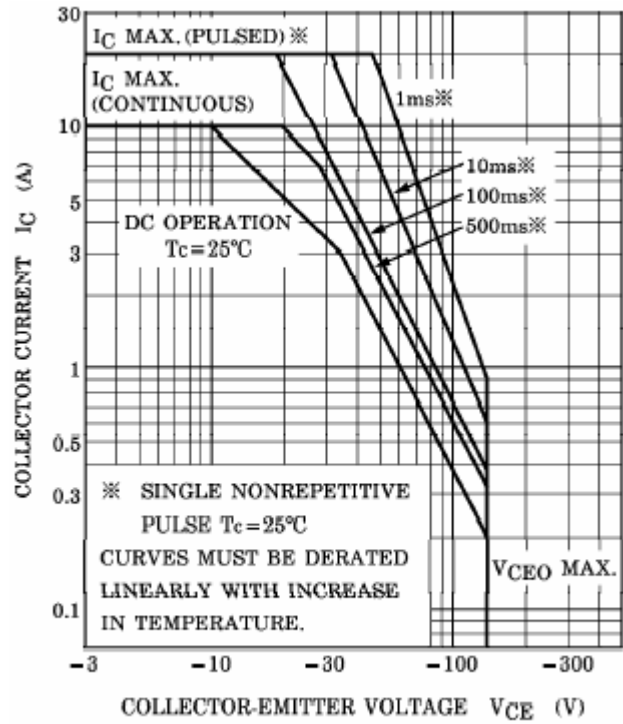


Fig.5 Safe Operating Area

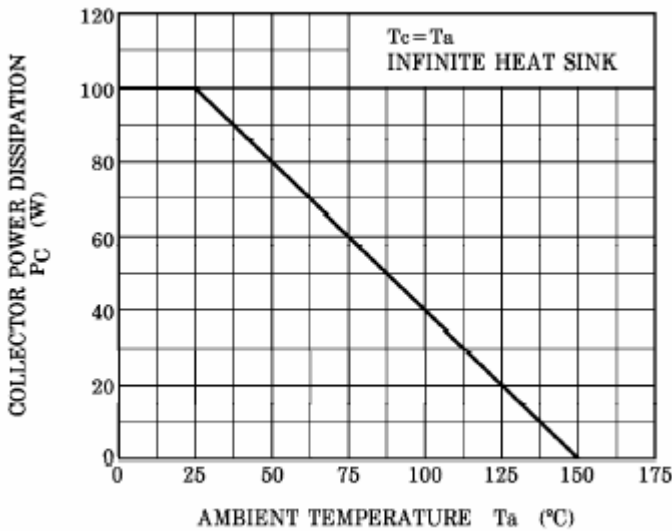


Fig.6 Pc-Ta Derating