MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6233
2N6235

HIGH VOLTAGE NPN SILICON TRANSISTORS

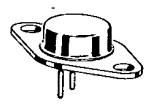
. . . useful for high-voltage medium power applications such as switching regulators.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 225 Vdc – 2N6233
  325 Vdc – 2N6235
- DC Current Gain – h_{FE} = 25 to 125 – I_C = 1.0 Adc
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- High Frequency Response – f_T = 20 MHz (Min)
- Fast Switching Times @ 1.0 Adc –
  t_r = 0.5 μs (Max)
  t_s = 3.5 μs (Max)
  t_f = 0.5 μs (Max)

5 AMPERE

POWER TRANSISTORS NPN SILICON

225,275,325 VOLTS
50 WATTS



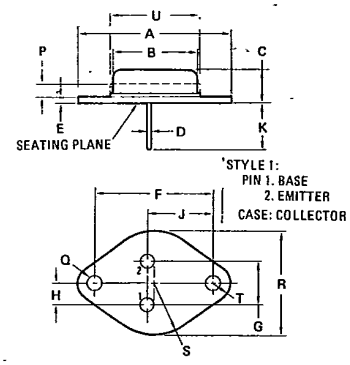
***MAXIMUM RATINGS**

Rating	Symbol	2N6233	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	325	Vdc
Collector-Base Voltage	V_{CB}	250	350	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data.

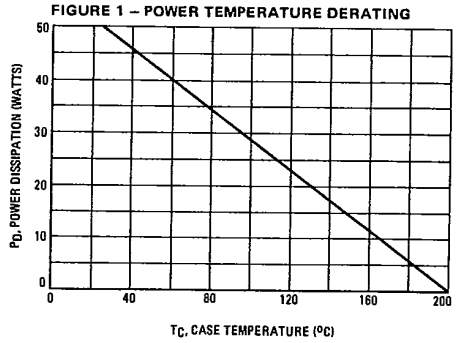


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA

FIGURE 1 – POWER TEMPERATURE DERATING



2N6233, 2N6235

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

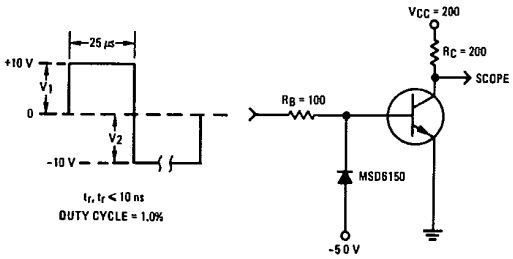
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 20 mAdc, I_B = 0)	2N6233 2N6235	$V_{CEO(sus)}$	225 325	— —	Vdc
Collector Cutoff Current (V_{CE} = 225, I_B = 0) (V_{CE} = 325, I_B = 0)	2N6233 2N6235	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6233 2N6235	I_{CEX}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0) (V_{CB} = 350 Vdc, I_E = 0)	2N6233 2N6235	I_{CBO}	— —	0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	25 25 10	— 125 —	—
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	— —	0.5 2.5	Vdc
Base Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	— —	1.0 2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	20	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	250	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_B = 0.1 Adc)		t_r	—	0.5	μs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_s	—	3.5	μs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)		t_f	—	0.5	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6 R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVEL; D_1 DISCONNECTED AND V_2 REDUCED TO 5 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 – TURN-ON TIME

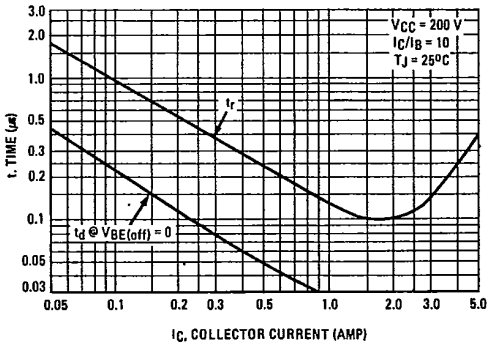


FIGURE 4 – THERMAL RESPONSE

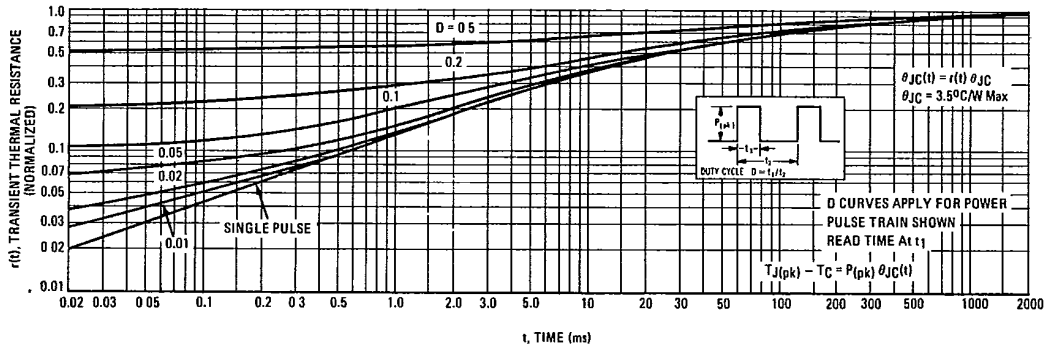
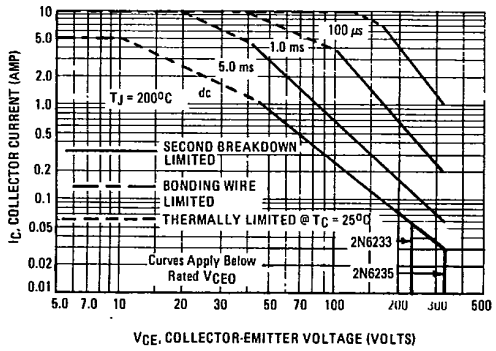


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

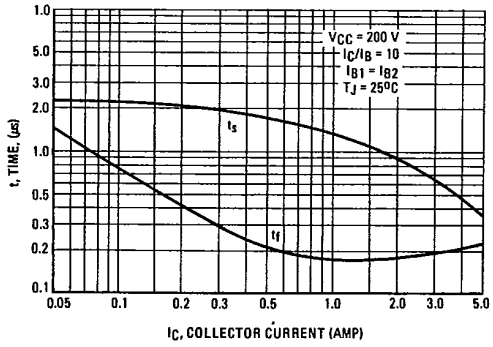
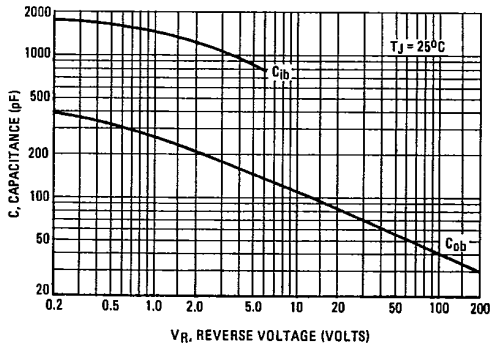



FIGURE 7 – CAPACITANCES