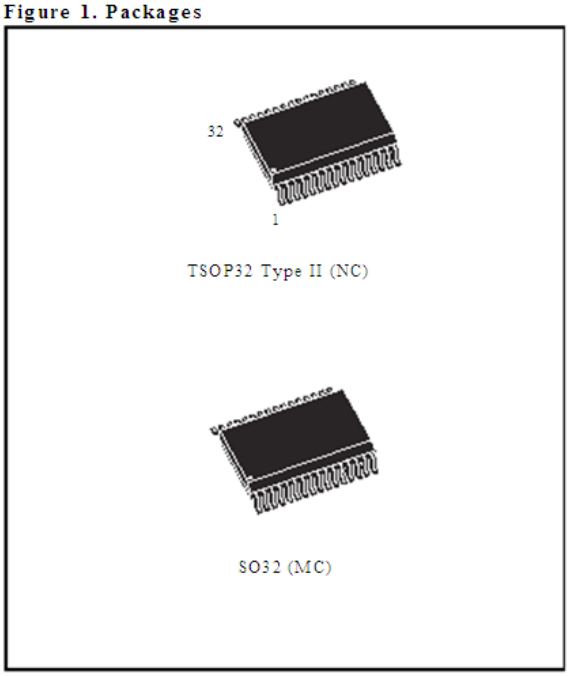
M68AF511A

4 Mbit (512K x8), 5V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 4.5 to 5.5V
- 512K x 8 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 55ns
- LOW STANDBY CURRENT
- LOW Vcc DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER

Figure 1. Packages



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SUMMARY DESCRIPTION

The M68AF511A is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 524,288 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 4.5 to 5.5V supply.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AF511A is available in a 32 lead TSOP Type II and 32 lead SO packages.

Figure 2. Logic Diagram

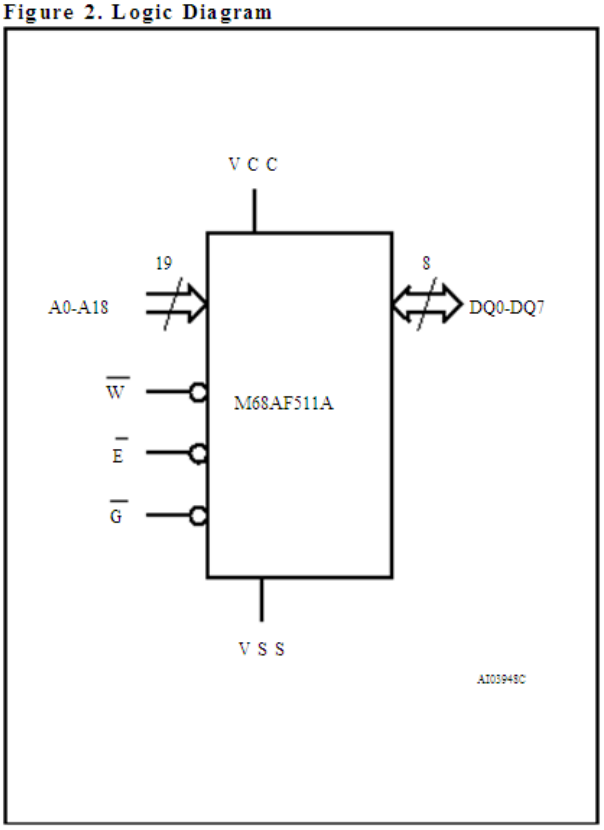


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
Vcc	Supply Voltage
Vss	Ground

Figure 3. TSOP and SO Connections

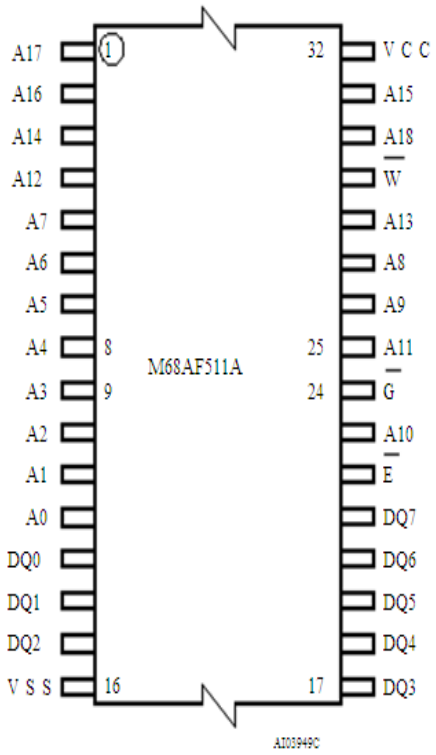
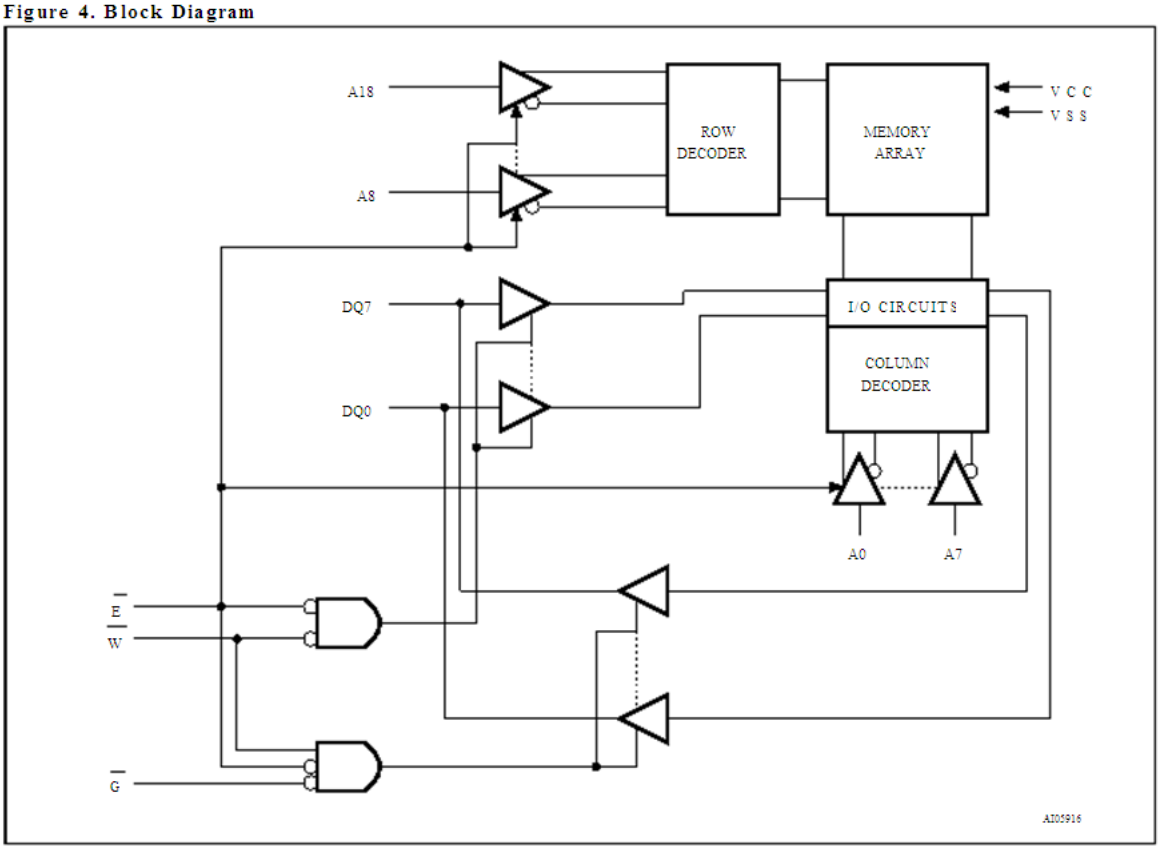


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for periods greater than 1 sec may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_O (1)	Output Current	20	mA
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.5 to 6.5	V
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 6.0V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter		M68AF511A
V_{CC} Supply Voltage		4.5 to 5.5V
Ambient Operating Temperature	Range 1: Commercial	0 to 70°C
	Range 6: Industrial	–40 to 85°C
Load Capacitance (CL)		100pF
Output Circuit Protection Resistance (R1)		3.0kΩ
Load Resistance (R2)		3.1kΩ
Input Rise and Fall Times		1ns/V
Input Pulse Voltages		0 to V_{CC}
Input and Output Timing Ref. Voltages		$V_{CC}/2$
Output Transition Timing Ref. Voltages		$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$

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P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 6.0V only.

OPERATION

The M68AF511A has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted (E = High). An Output Enable (G) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs W and E as summarized in the Operating Modes table (Table 6).

Table 6. Operating Modes

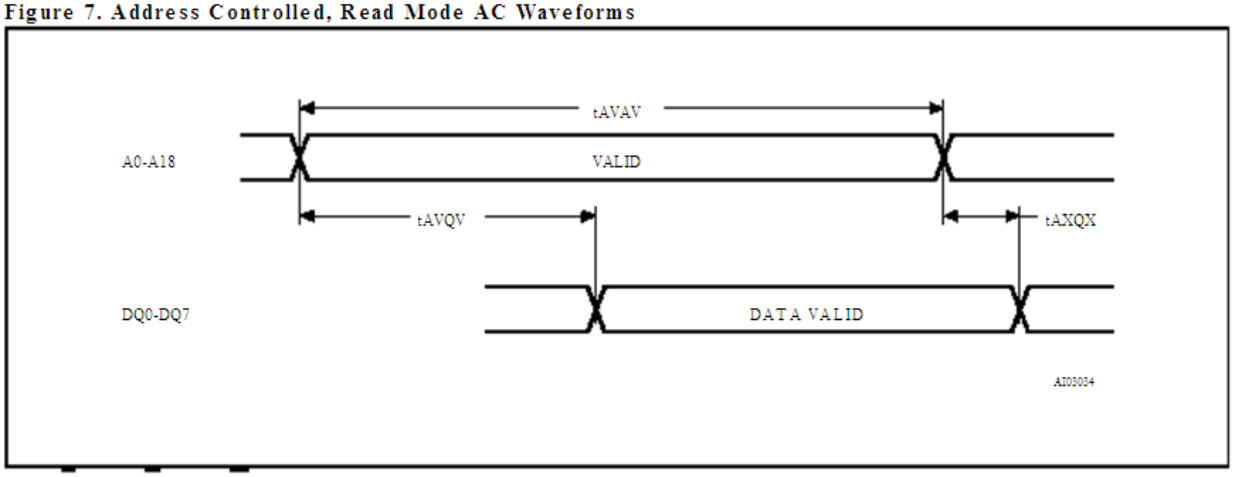
Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Output disabled	V_{IL}	X V_{IH}		Hi-Z	Active (ICC)
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active (ICC)
Write	V_{IL}	V_{IL}	X	Data Input	Active (ICC)
Deselect	V_{IH}	X	X	Hi-Z	Standby (ISB)

Note: X = V_{IH} or V_{IL}.

Read Mode

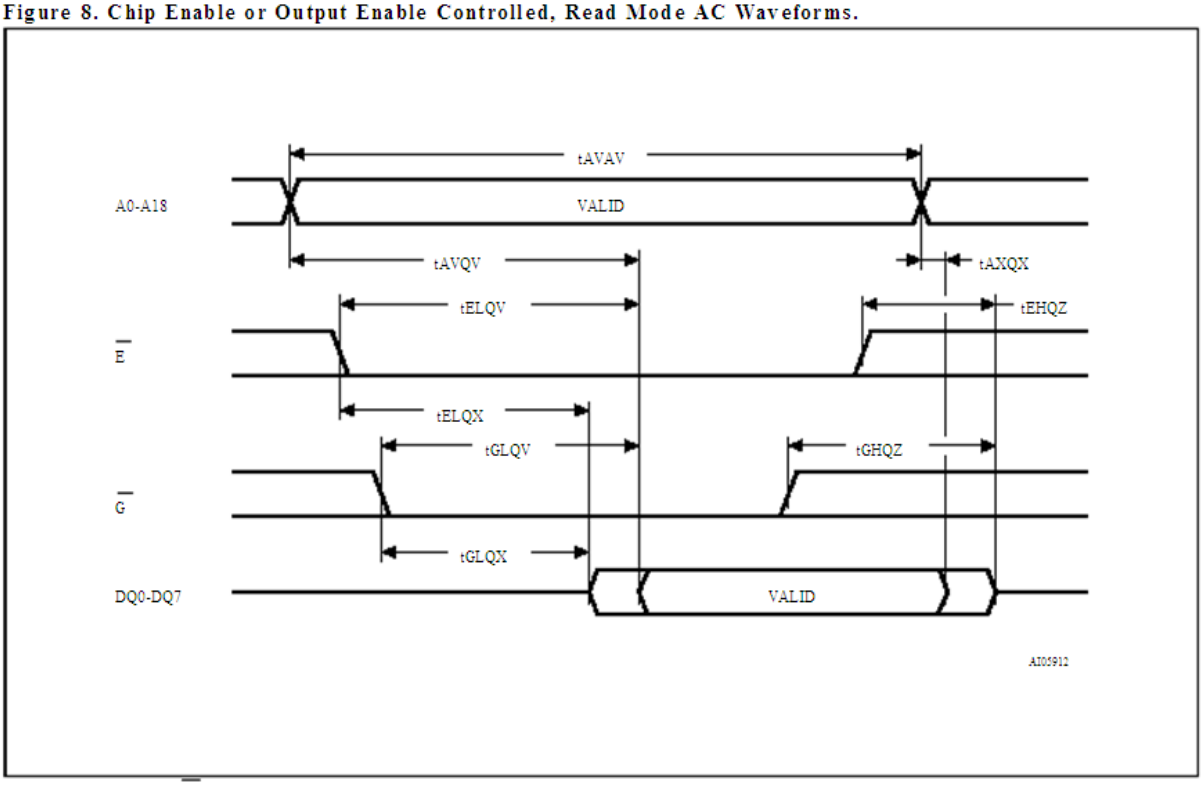
The M68AF511A is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted. This provides access to data from eight of the 4,194,304 locations in the static memory array, specified by the 19 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing G is Low and E is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: E = Low, G = Low, W = High.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable ($\overline{W}$) = High.

Figure 9. Chip Enable Controlled, Standby Mode AC Waveforms

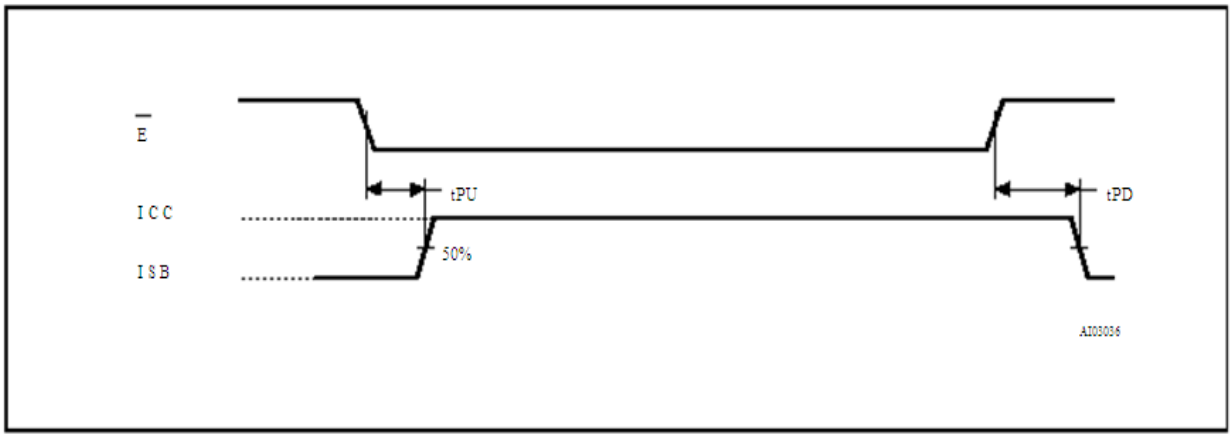


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter	M68AF511A			Unit
			55	70	
tAVAV	Read Cycle Time	Min	55	70	ns
tAVQV	Address Valid to Output Valid	Max	55	70	ns
tAXQX (1)	Data hold from Address change	Min	5	5	ns
tEHQZ (2,3)	Chip Enable High to Output Hi-Z	Max	20	25	ns
tELQV	Chip Enable Low to Output Valid	Max	55	70	ns
tELQX (1)	Chip Enable Low to Output Transition	Min	5	5	ns
tGHQZ (2,3)	Output Enable High to Output Hi-Z	Max	20	25	ns
tGLQV	Output Enable Low to Output Valid	Max	25	35	ns
tGLQX (1)	Output Enable Low to Output Transition	Min	5	5	ns
tPD (4)	Chip Enable High to Power Down	Max	0	0	ns
tPU (4)	Chip Enable Low to Power Up	Min	55	70	ns

Note: 1. Test conditions assume transition timig reference level = 0.3VCC or 0.7VCC.
2. At any given temperature and voltage condition, tEHQZ is less than tELQX and tGHQZ is less than tGLQX for any given device.
3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
4. Tested initially and after any design or process changes that may affect these parameters

Write Mode

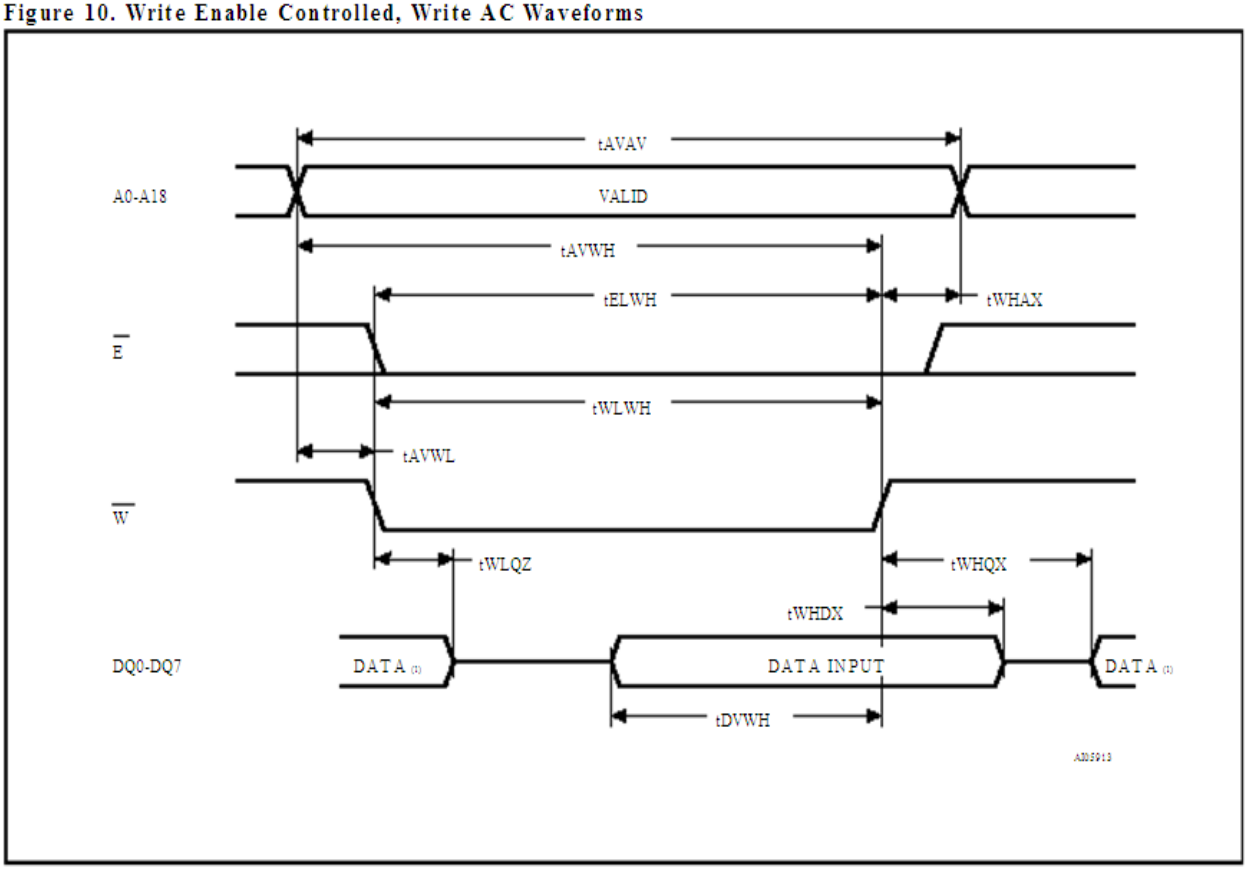
The M68AF511A is in the Write mode whenever the W and E pins are Low. Either the Chip Enable input (E) or the Write Enable input (W) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of Chip Enable being active with W low. Therefore, address setup time is referenced to Write Enable and Chip Enable as t_{AVWL} and t_{AVEH} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of E, or W.

if the Output is enabled (E = Low and G = Low), then W will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation.

Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of E, whichever occurs first, and remain valid for t_{WHDX} or t_{EHDX}.

Figure 10. Write Enable Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ7 are in output state and input signal should not be applied.

Figure 11. Chip Enable Controlled, Write AC Waveforms

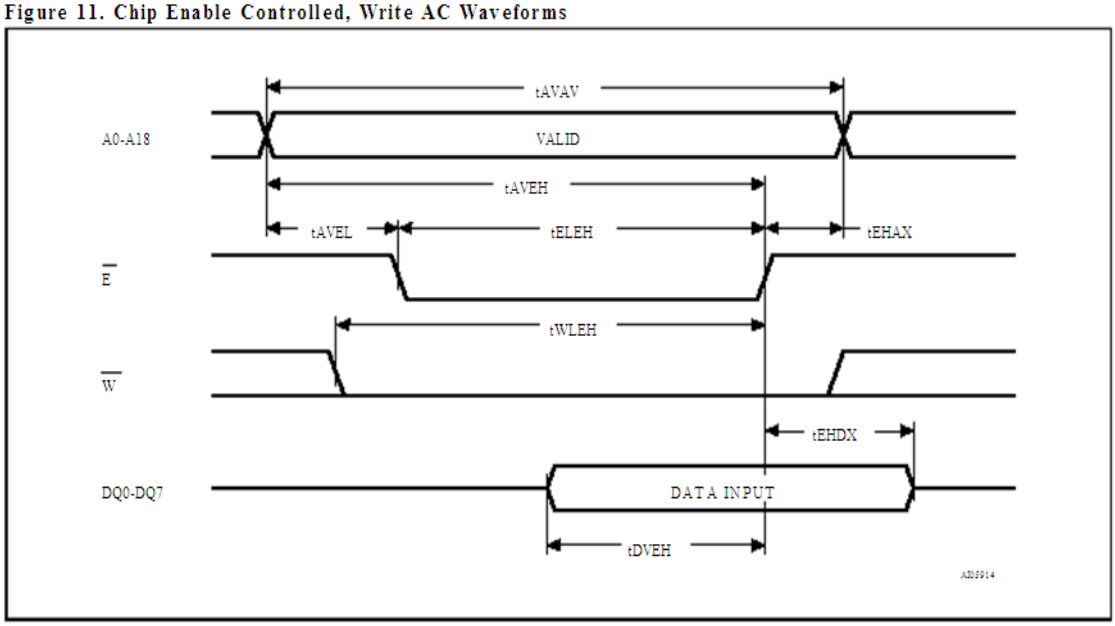


Table 8. Write Mode AC Characteristics

Symbol	Parameter	M68AF511A			Unit
			55	70	
tAVAV	Write Cycle Time	Min	55	70	ns
tAVEH	Address Valid to Chip Enable High	Min	45	60	ns
tAVEL	Address Valid to Chip Enable Low	Min	0	0	ns
tAVWH	Address Valid to Write Enable High	Min	45	60	ns
tAVWL	Address Valid to Write Enable Low	Min	0	0	ns
tDVEH	Input Valid to Chip Enable High	Min	25	30	ns
tDVWH	Input Valid to Write Enable High	Min	25	30	ns
tEHAX	Chip Enable High to Address Transition	Min	0	0	ns
tEHDX	Chip Enable High to Input Transition	Min	0	0	ns
tELEH	Chip Enable Low to Chip Enable High	Min	45	60	ns
tELWH	Chip Enable Low to Write Enable High	Min	45	60	ns
tWHAX	Write Enable High to Address Transition	Min	0	0	ns
tWHDX	Write Enable High to Input Transition	Min	0	0	ns
tWHQX (1)	Write Enable High to Output Transition	Min	5	5	ns
tWLEH	Write Enable Low to Chip Enable High	Min	45	60	ns
tWLQZ (1,2)	Write Enable Low to Output Hi-Z	Max	20	25	ns
tWLWH	Write Enable Low to Write Enable High	Min	45	60	ns

Note: 1. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.

Figure 12. Low VCC Data Retention AC Waveforms.

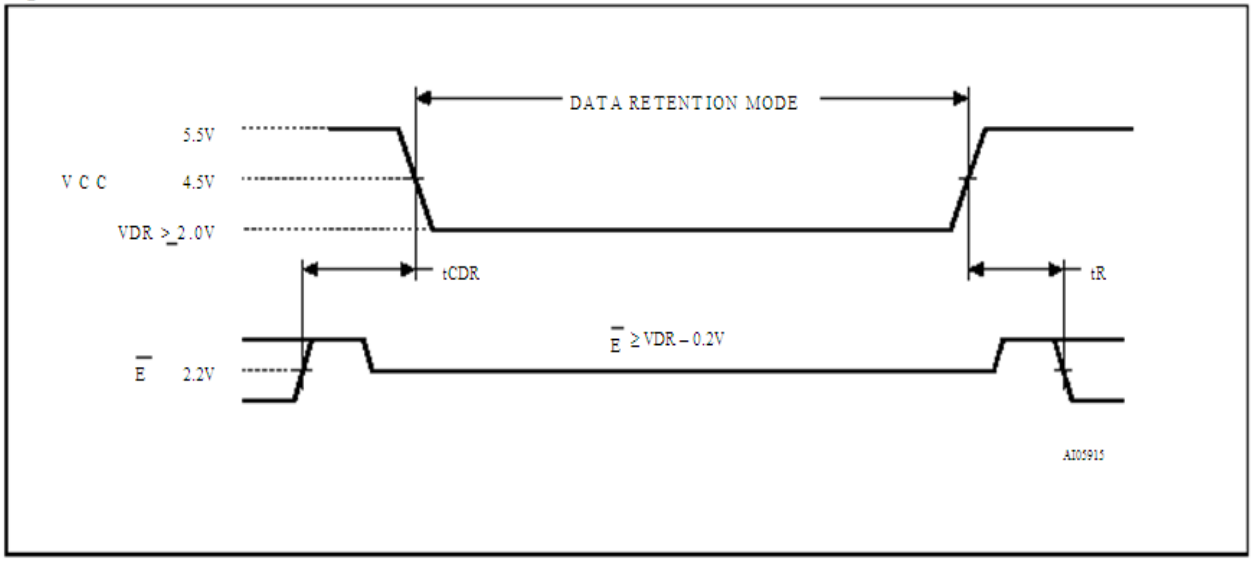


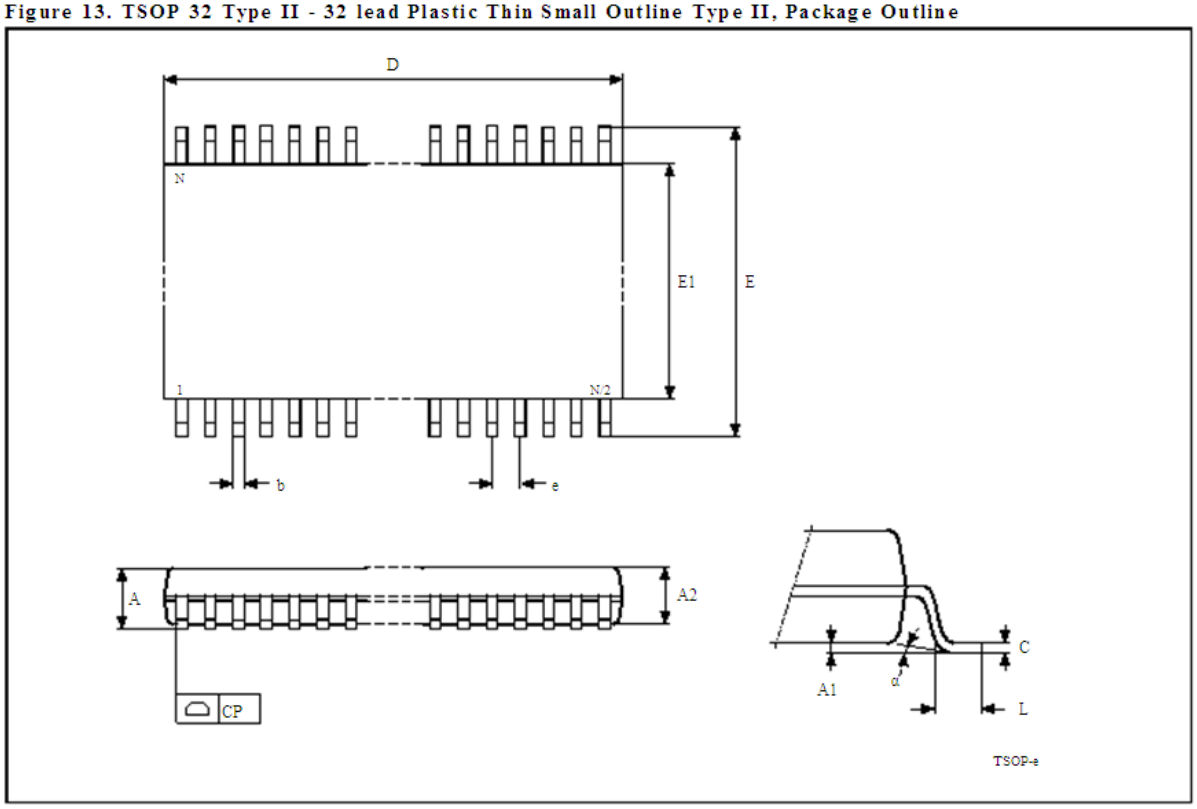
Table 9. Low VCC Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 2V, E ≥ V_{CC} – 0.2V, f = 0 (3)		4.5	9	µA
t_{CDR} (1,2)	Chip Deselected to Data Retention Time		0	n s		
t_R (2)	Operation Recovery Time		tAVAV			ns
V_{DR} (2)	Supply Voltage (Data Retention)	Ē ≥ V_{CC} – 0.2V, f = 0	2V			

Note: 1. All other Inputs at $V_{IH} \geq V_{CC}$ –0.2V or $V_{IL} \leq$ 0.2V.
2. Tested initially and after any design or process that may affect these parameteres. tAVAV is Read cycle time.
3. No input may exceed V_{CC} +0.2V.

PACKAGE MECHANICAL

Figure 13. TSOP 32 Type II - 32 lead Plastic Thin Small Outline Type II, Package Outline

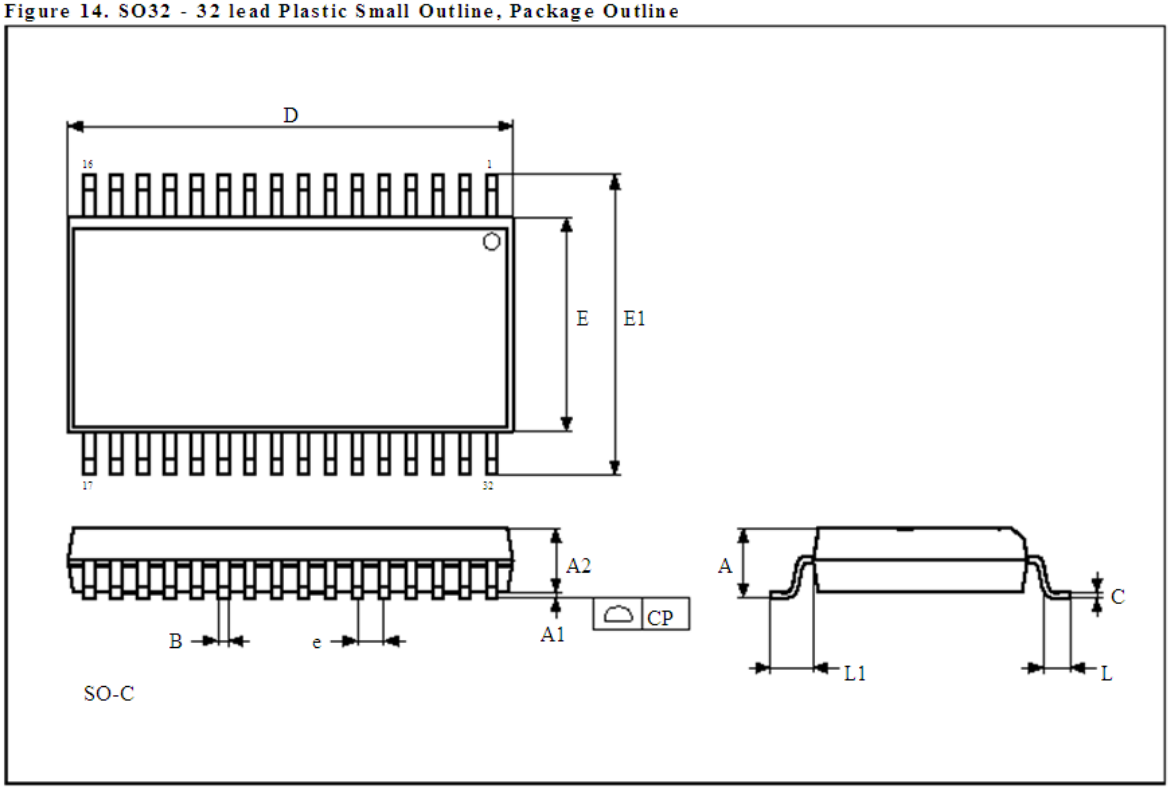


Note: Drawing is not to scale.

Table 10. TSOP 32 Type II - 32 lead Plastic Thin Small Outline Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
b		0.30	0.52		0.012	0.020
C		0.12	0.21		0.005	0.008
CP			0.10			0.004
D		20.82	21.08		0.820	0.830
e	1.27	–	–	0.050	–	–
E		11.56	11.96		0.455	0.471
E1		10.03	10.29		0.395	0.405
L		0.40	0.60		0.016	0.024
α		0°	5°		0°	5°
N 3	2			32		

Figure 14. SO32 - 32 lead Plastic Small Outline, Package Outline



Note: Drawing is not to scale.

Table 11. SO32 - 32 lead Plastic Small Outline, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.00			0.118
A1		0.10			0.004	
A2		2.57	2.82		0.101	0.111
B		0.36	0.51		0.014	0.020
C		0.15	0.30		0.006	0.012
D		20.14	20.75		0.793	0.817
E		11.18	11.43		0.440	0.450
E1		13.87	14.38		0.546	0.566
e	1.27	–	–	0.050	–	–
L		0.58	0.99		0.023	0.039
L1		1.19	1.60		0.047	0.063
CP			0.10			0.004