

## Description

The μPD4464 is a high-speed 8,192-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Full CMOS storage cells with six transistors make the μPD4464 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is included for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 volts.

The μPD4464 is available in standard 28-pin plastic DIP or miniflat packaging.

## Features

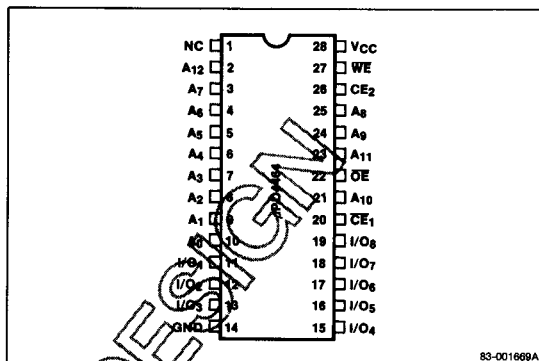
- Operating temperature range: -40 to 85 °C
- Single +5-volt power supply
- Fully static operation — no clock or refreshing required
- TTL-compatible inputs and outputs
- Common I/O using three-state output
- One output enable pin and two chip enable pins for easy application
- Data retention voltage: 2 V minimum
- Standard 28-pin plastic DIP or miniflat packaging

## Ordering Information

Part Number	Access Time (max)	Active Current (max)	Standby Current (max)	Package
μPD4464C-12	120 ns	40 mA	10 μA	28-pin plastic DIP
C-15	150 ns	40 mA		
C-20	200 ns	35 mA		
μPD4464C-12L	120 ns	40 mA	1 μA (at T <sub>A</sub> = 60°C)	28-pin plastic DIP
C-15L	150 ns	40 mA		
C-20L	200 ns	35 mA		
μPD4464G-12	120 ns	40 mA	10 μA	28-pin plastic miniflat
G-15	150 ns	40 mA		
G-20	200 ns	35 mA		
μPD4464G-12L	120 ns	40 mA	1 μA (at T <sub>A</sub> = 60°C)	28-pin plastic miniflat
G-15L	150 ns	40 mA		
G-20L	200 ns	35 mA		

## Pin Configuration

### 28-Pin Plastic DIP or Miniflat



## Pin Identification

Symbol	Function
A <sub>0</sub> -A <sub>12</sub>	Address inputs
I/O <sub>1</sub> -I/O <sub>8</sub>	Data inputs/outputs
CE <sub>1</sub>	Chip enable (active low)
CE <sub>2</sub>	Chip enable (active high)
OE	Output enable
WE	Write enable
GND	Ground
V <sub>CC</sub>	+5-volt power supply
NC	No connection

## Absolute Maximum Ratings

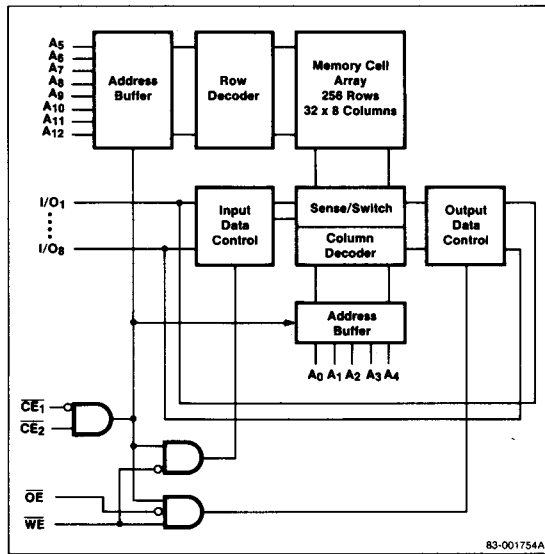
Power supply voltage, V <sub>CC</sub> (Note 1)	-0.5 to +7.0 V
Input voltage, V <sub>IN</sub> (Note 1)	-0.5 to V <sub>CC</sub> + 0.5 V
Output voltage, V <sub>OUT</sub> (Note 1)	-0.5 to V <sub>CC</sub> + 0.5 V
Operating temperature, T <sub>OPR</sub>	-40 to 85 °C
Storage temperature, T <sub>STG</sub>	-55 to 125 °C
Power dissipation, P <sub>D</sub>	1.0 W

### Notes:

(1) -3.0 V minimum (pulse width = 50 ns maximum)

**Comment:** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

## Block Diagram



83-001754A

## Recommended DC Operating Conditions

$T_A = -40$  to  $85^\circ\text{C}$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage, low (Note 1)	$V_{IL}$	-0.3		0.8	V
Input voltage, high	$V_{IH}$	2.2		$V_{CC} + 0.5$	V

### Notes:

(1) -3.0 V minimum (pulse width = 50 ns maximum)

## Capacitance

$T_A = 25^\circ\text{C}$ ;  $f = 1.0$  MHz

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	$C_{IN}$			6	pF	$V_{IN} = 0$ V
I/O capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

## DC Characteristics

$T_A = -40$  to  $85^\circ\text{C}$ ;  $V_{CC} = +5.0$  V  $\pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input leakage current	$I_{LI}$			1	$\mu\text{A}$	$V_{IN} = 0$ V to $V_{CC}$
I/O leakage current	$I_{LO}$			1	$\mu\text{A}$	$V_{I/O} = 0$ V to $V_{CC}$ ; $\overline{CE}_1 = V_{IH}$ or $\overline{CE}_2 = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	$I_{CCA1}$			40	mA	$\overline{CE} = V_{IL}$ ; $\overline{CE}_2 = V_{IH}$ ; $I_{I/O} = 0$ (min cycle)
				(Note 1)		
Standby supply current	$I_{CCS1}$			0.004	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2$ V; $\overline{CE}_2 \geq V_{CC} - 0.2$ V
				(Note 2)		
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 2.1$ mA
				2.4		
Output voltage, high	$V_{OH}$				V	$I_{OH} = -1.0$ mA
Operating supply current	$I_{CCA2}$			5	mA	$\overline{CE} = V_{IL}$ ; $\overline{CE}_2 = V_{IH}$ ; $I_{I/O} = 0$ (dc current)
				10		
Standby supply current	$I_{CCS2}$			0.004	$\mu\text{A}$	$\overline{CE}_2 \leq 0.2$ V
				(Note 2)		

### Notes:

(1)  $\mu\text{PD4464-20/-20L}$ : 35 mA max

(2)  $\mu\text{PD4464-12L/-15L/-20L}$ : 1.0  $\mu\text{A}$  max ( $-40$  to  $60^\circ\text{C}$ )  
0.2  $\mu\text{A}$  max ( $-40$  to  $25^\circ\text{C}$ )

## Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	$I_{CC}$
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	$D_{OUT}$ disabled	High-Z	Active
L	H	L	H	Read	$D_{OUT}$	Active
L	H	X	L	Write	$D_{IN}$	Active

### Notes:

(1) X = don't care

### AC Characteristics

T<sub>A</sub> = -40 to 85°C; V<sub>CC</sub> = +5.0 V ±10%

Parameter	Symbol	Limits						Unit	Test Conditions (Note 1)
		μPD4464-12		μPD4464-15		μPD4464-20			
		Min	Max	Min	Max	Min	Max		
<b>Read Cycle</b>									
Read cycle time	t <sub>RC</sub>	120		150		200		ns	
Address access time	t <sub>AA</sub>		120		150		200	ns	
$\overline{CE}_1$ access time	t <sub>CO1</sub>		120		150		200	ns	
CE <sub>2</sub> access time	t <sub>CO2</sub>		120		150		200	ns	
Output enable to output valid	t <sub>OE</sub>		60		75		100	ns	
Output hold from address change	t <sub>OH</sub>	10		10		10		ns	
Chip enable ( $\overline{CE}_1$ ) to output in low-Z	t <sub>LZ1</sub>	10		10		100		ns	
Chip enable (CE <sub>2</sub> ) to output in low-Z	t <sub>LZ2</sub>	10		10		10		ns	
Output enable to output in low-Z	t <sub>OLZ</sub>	5		5		5		ns	
Chip enable ( $\overline{CE}_1$ ) to output in high-Z	t <sub>HZ1</sub>		40		75		100	ns	
Chip enable (CE <sub>2</sub> ) to output in high-Z	t <sub>HZ2</sub>		40		75		100	ns	
Output enable to output in high-Z	t <sub>OHZ</sub>		40		60		80	ns	
<b>Write Cycle</b>									
Write cycle time	t <sub>WC</sub>	120		150		200		ns	
Chip enable ( $\overline{CE}_1$ ) to end of write	t <sub>CW1</sub>	85		130		180		ns	
Chip enable (CE <sub>2</sub> ) to end of write	t <sub>CW2</sub>	85		130		180		ns	
Address valid to end of write	t <sub>AW</sub>	85		130		180		ns	
Address setup time	t <sub>AS</sub>	0		0		0		ns	
Write pulse width	t <sub>WP</sub>	70		100		140		ns	
Write recovery time	t <sub>WR</sub>	5		5		5		ns	
Data valid to end of write	t <sub>DW</sub>	50		70		80		ns	
Data hold time	t <sub>DH</sub>	5		5		5		ns	
Write enable to output in high-Z	t <sub>WHZ</sub>		40		75		100	ns	
Output active from end of write	t <sub>OW</sub>	5		10		10		ns	

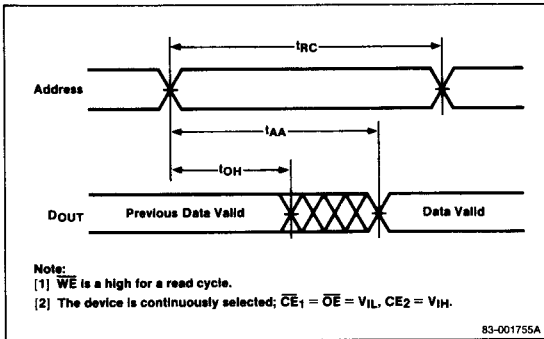
**Notes:**

- (1) Input pulse levels = 0.8 V to 2.4 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; output load = 1 TTL gate and C<sub>L</sub> = 100 pF.

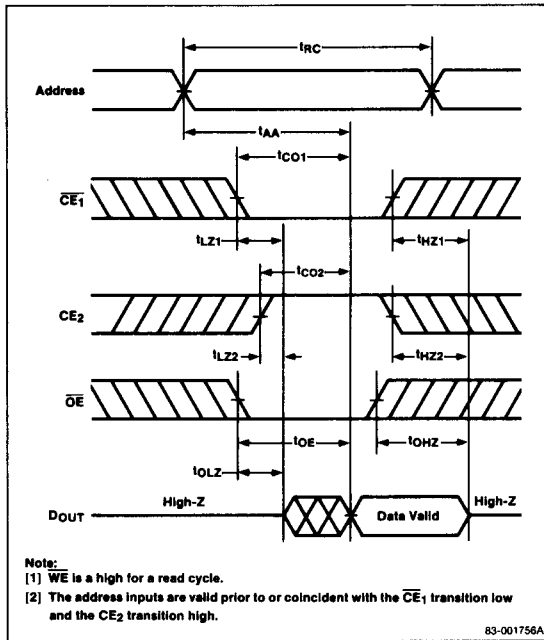
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**Timing Waveforms**

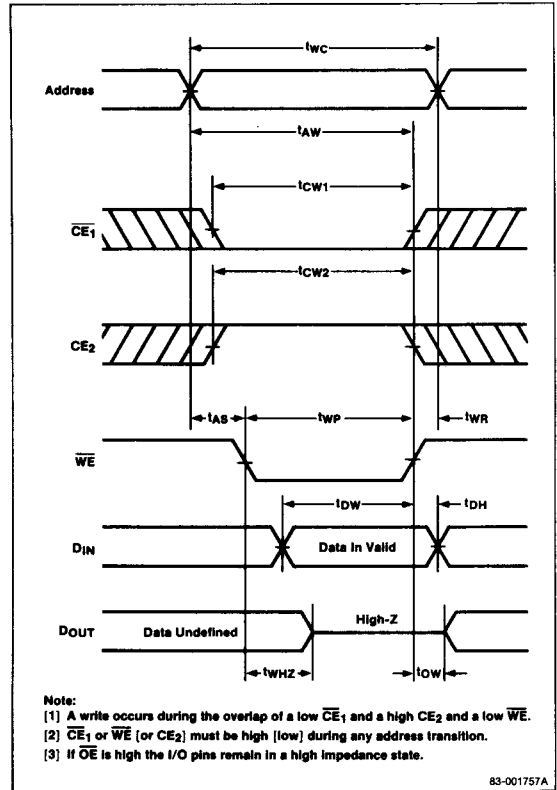
**Read Cycle No. 1 (Address Access)**



**Read Cycle No. 2 (Chip Enable Access)**

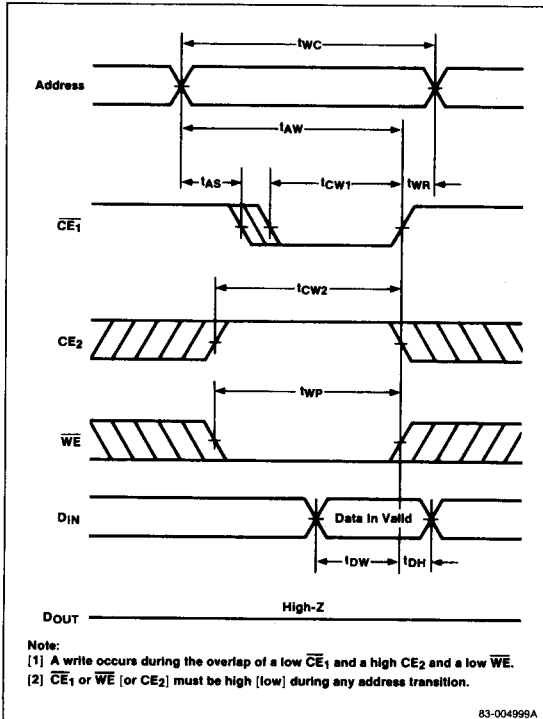


**Write Cycle No. 1 ( $\overline{WE}$ -Controlled)**

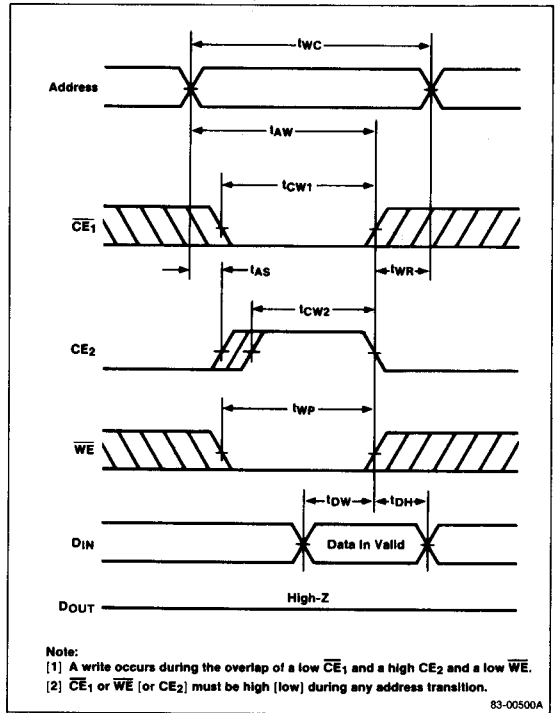


## Timing Waveforms (cont)

### Write Cycle No. 2 ( $\overline{CE}_1$ -Controlled)



### Write Cycle No. 3 ( $\overline{CE}_2$ -Controlled)



## Low V<sub>CC</sub> Data Retention Characteristics

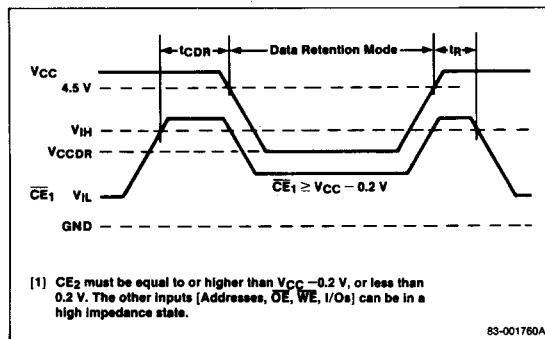
T<sub>A</sub> = -40 to 85°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data retention supply voltage	V <sub>CCDR1</sub>	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V};$ $CE_2 \geq V_{CC} - 0.2 \text{ V}$
	V <sub>CCDR2</sub>	2.0		5.5	V	$CE_2 \leq 0.2 \text{ V}$
Data retention supply current	I <sub>CCDR1</sub>	0.003	10		μA	$V_{CC} = 3.0 \text{ V};$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V};$ $CE_2 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$
	I <sub>CCDR2</sub>	0.003	10		μA	$V_{CC} = 3.0 \text{ V};$ $CE_2 \leq 0.2 \text{ V}$
Chip deselect to data retention time	t <sub>CDR</sub>	0			ns	
Operation recovery time	t <sub>R</sub>		t <sub>RC</sub>		ns	

**Notes:**

- (1) μPD4464-12L/-15L/-20L: 1.0 μA max (-40 to 60°C)  
0.2 μA max (-40 to 25°C)

## Data Retention ( $\overline{CE}_1$ -Controlled)



## Data Retention (CE<sub>2</sub>-Controlled)

