

Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator

FEATURES

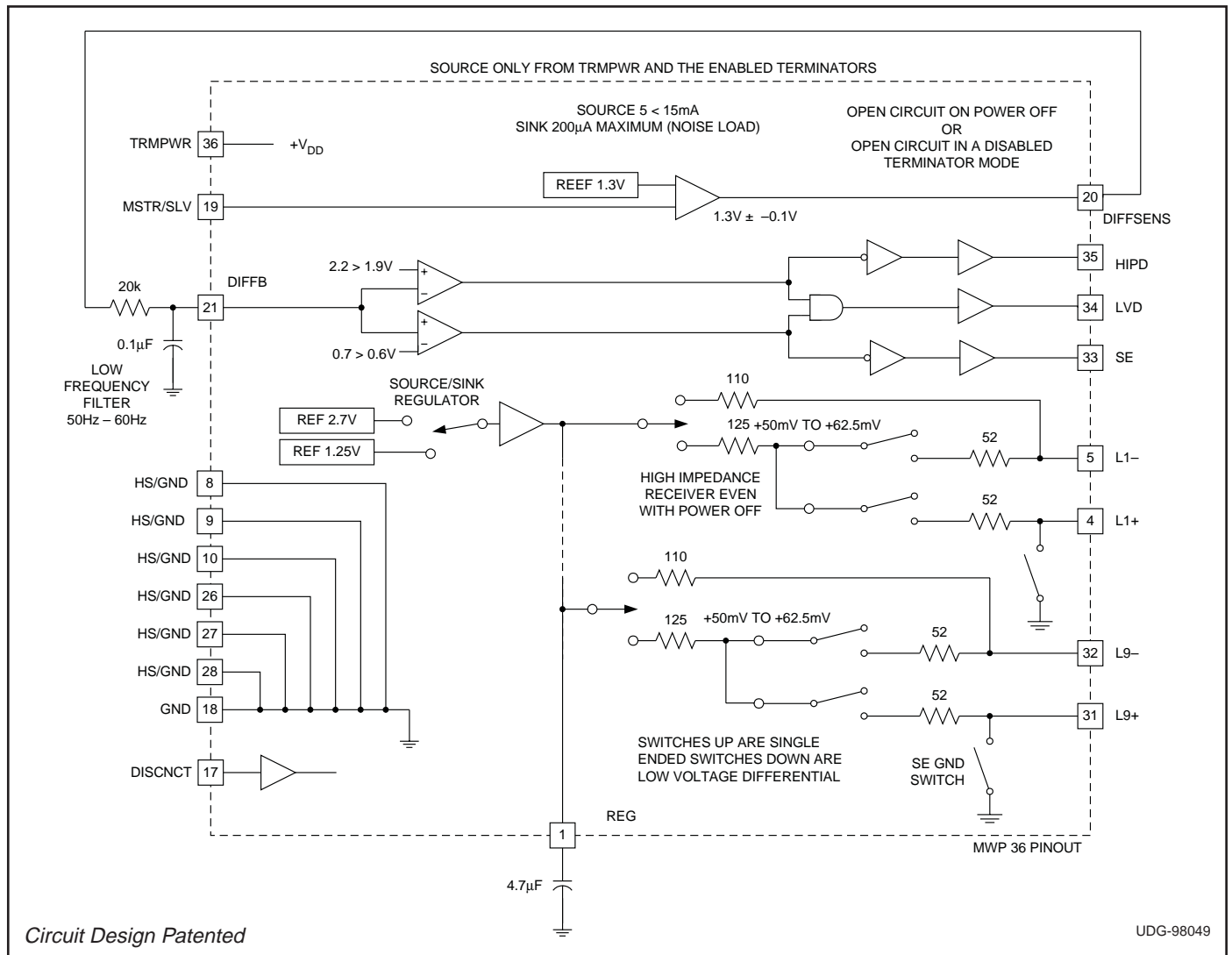
- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF
- Master/Slave Inputs
- Supports Active Negation
- Standby (Disable Mode) 5µA
- 3pF Channel Capacitance

DESCRIPTION

The UCC5630 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for Fast-40 and Fast-80, but has the potential of speeds up to Fast-320. The UCC5630 is SPI-2, SPI and Fast-20 compliant. Consult SSOP-36 and LQFP-48 Package Diagram for exact dimensions.

The UCC5630 can not be used with SCSI high voltage differential (HVD) EIA485. It will shut down when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD or single ended and the bias voltage, current and power are also different for EIA485 differential.

BLOCK DIAGRAM

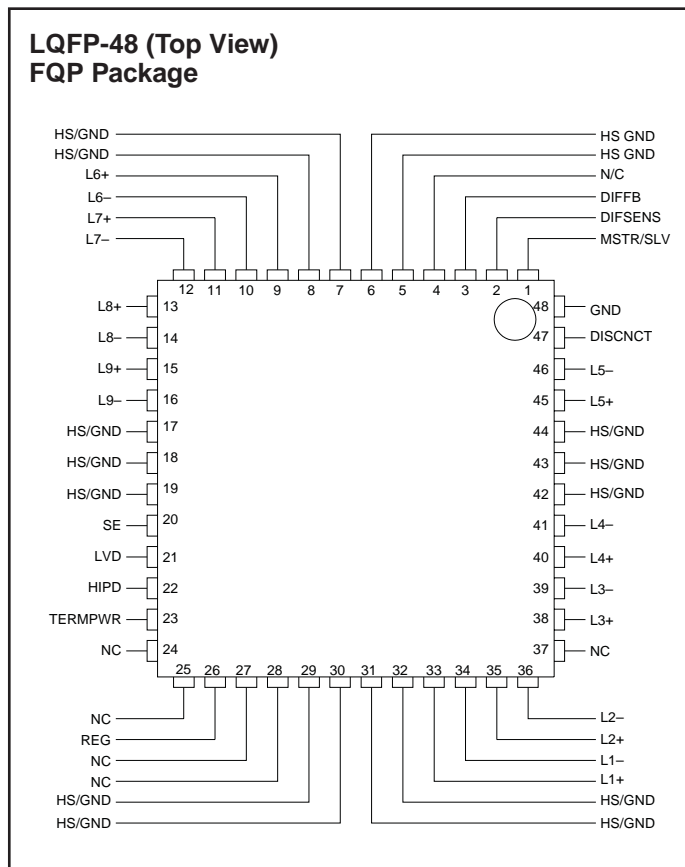
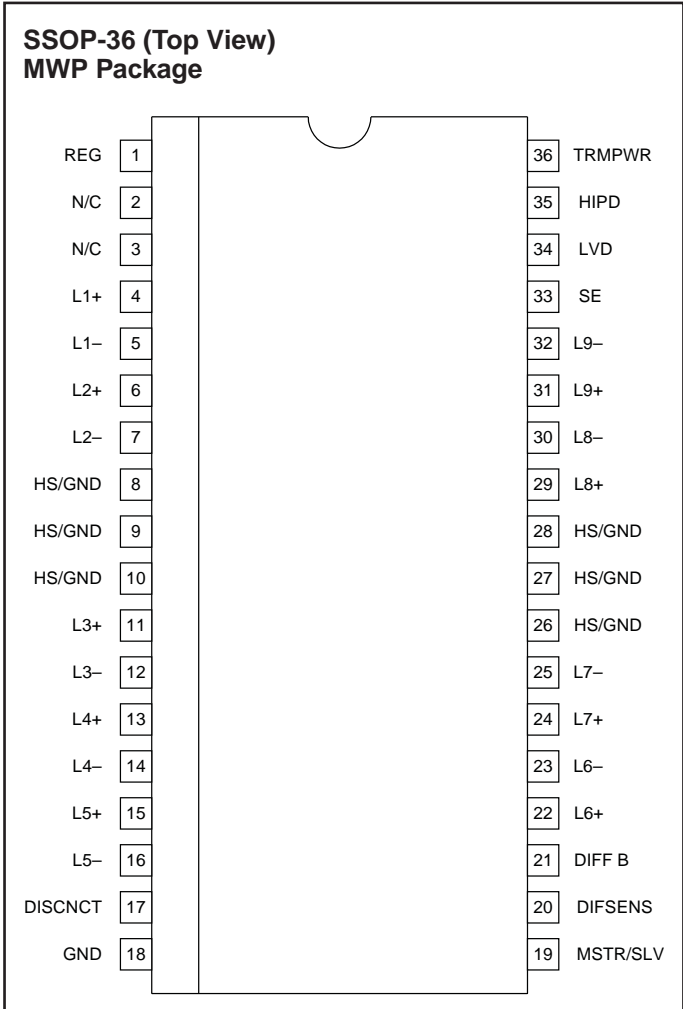


ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
 Signal Line Voltage 0V to TRMPWR
 Package Power Dissipation 2W
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10sec.) +300°C

All voltages are with respect to PIN1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage 2.7V TO 5.25V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current				20	mA
	Disable Terminator, in DISCNCT mode.			35	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	LVD Mode, Differential Sense Floating	-80	-100		mA
1.25V Regulator Sink Current	LVD Mode, Differential Sense Floating	80	100		mA
1.3V Regulator	DIFSENS	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFSENS	-5		-15	mA
1.3V Regulator Sink Current	DIFSENS	50		200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, $T_A = 0^\circ\text{C}$ to 70°C , $\text{TRMPWR} = 3.3\text{V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
2.7V Regulator	Single Ended Mode	2.5	2.7	3	V
2.7V Regulator Source Current	Single Ended Mode	-200	-400	-800	mA
2.7V Regulator Sink Current	Single Ended Mode	100	200	400	mA
2.7V Regulator Dropout Voltage	$V_{\text{TRMPWR}} - (V_{\text{REG}} - 2.7 \text{ Min})$			200	mV
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance		110	125	165	Ω
Differential Bias Voltage	Drivers Tri-stated	100		125	mV
Common Mode Bias			1.25		V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3.5	pF
Single Ended Termination Section					
Impedance		102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V	-21	-23	-25.4	mA
	Signal Level 0.5V			-22.4	mA
Output Leakage	Disabled, $\text{TRMPWR} = 0\text{V}$ to 5.25V			400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SW Impedance				60	Ω
Disconnect (DISCNET) Input Section					
DISCNET Threshold		0.8		2.0	V
DISCNET Input Current	$V_{\text{DISCNET}} = 0\text{V}$ and 3.3V	-30		30	μA
Differential Sense (DIFFB) Input Sections					
DIFFB Single Ended Threshold		0.6		0.7	V
DIFFB Sense LVDS Threshold		1.9		2.2	V
DIFFB Input Current	$V_{\text{DIFFB}} = 0\text{V}$ and 3.3V	-30		30	μA
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold		0.8		2	V
MSTR/SLV Input Current		-30		30	μA
Status Bits (SE, LVD, HIPD) Output Section					
I_{SOURCE}	$V_{\text{LOAD}} = 2.4\text{V}$	-4	-8.7		mA
I_{SINK}	$V_{\text{LOAD}} = 0.5\text{V}$	3	6		mA
	$V_{\text{LOAD}} = 0.4\text{V}$	2	5		mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

DIFFB: DIFSENS filter pin should be connected to a $0.1\mu\text{F}$ capacitor to GND and 20k resistor to SCSI/Bus DIFSENS Line.

DIFSENS: The SCSI bus DIFSENS line is driven to 1.3V to detect what type of devices are connected to the SCSI bus.

DISCNET: Disconnect shuts down the terminator when it is not at the ended of the bus. The disconnect pin low enables the terminator.

HIPD: TTL compatible status bit indicating high voltage differential has been detected on DIFFB. The terminator

is in shutdown. (Not valid in disconnect mode.)

HS/GND: Heat Sink GND. Connect to large area PC board traces to increase power dissipation capability.

GND: Power Supply Return.

L1- thru L9-: Signal line/active line for single ended or negative line in differential applications for the SCSI bus.

L1+ thru L9+: Ground line for single ended or positive line for differential applications for the SCSI bus.

LVD: TTL compatible status bit indicating low voltage differential level on DIFFB. The terminator is in LVD mode. (Not valid in disconnect mode.)

PIN DESCRIPTIONS (cont.)

MSTR/SLV: Mode select for the non-controlling terminator. MSTR enables the 1.3V regulator, when the terminator is enabled. Note: This function will be removed on further generations of the multimode terminators.

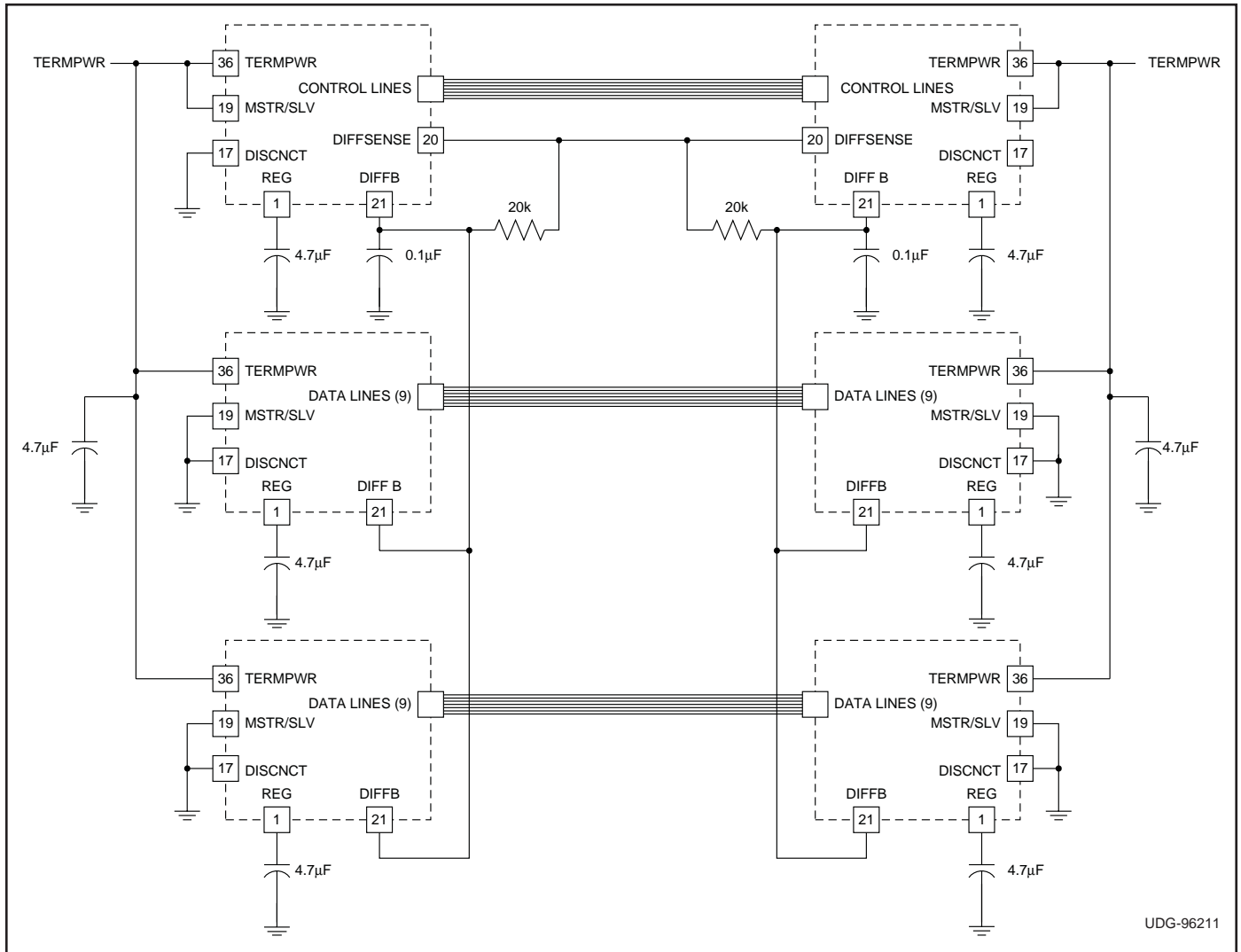
REG: Regulator bypass, must be connected to a 4.7μF

capacitor.

SE: TTL compatible status bit indicating single ended device has been detected on DIFFB. The terminator is in single ended mode.

TRMPWR: VIN 2.7V to 5.25V supply.

APPLICATION INFORMATION



Balancing capacitor is very important in high speed operation. The typical balance between the positive (+) and negative (-) signals is 0.1pF except for L8 and L9, 0.23pF and 0.4pF respectively on the MWP package. The negative (-) signal has higher capacitance than the positive (+) signal. The FQP package is typically 0.2pF less than the MWP. Typical balance is 0.1pF except for L8 and L3, where it is 0.4pF.

The master is selected by placing TRMPWR on MSTR/SLV and the terminator enabled by grounding DISCNCT, enabling the 1.3V regulator. The master is the only terminator connected directly to DIFSENS bus line, all the other terminators receive the mode signal by connecting the DIFFB pins together.

Note: The Master/Slave function will not be on future terminators.

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