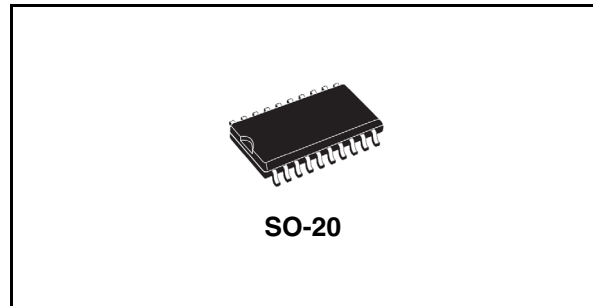


Combo IC for PFC and ballast control

Features

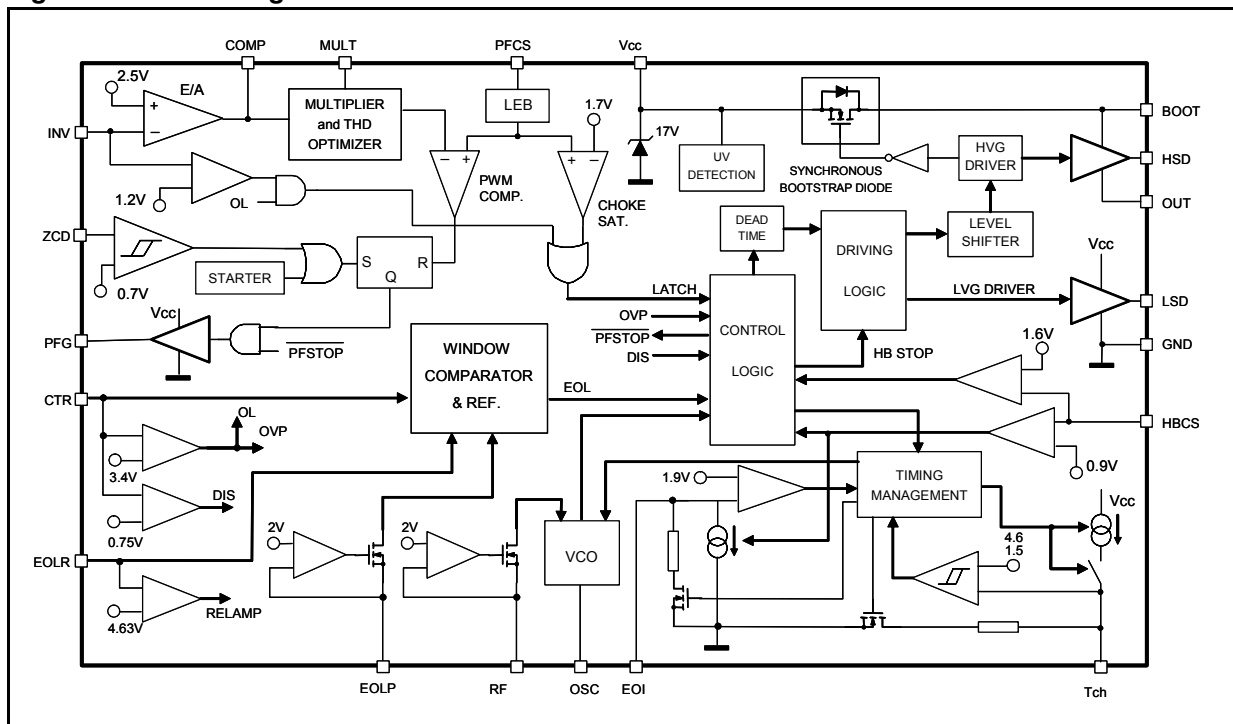
- Pre-heating and ignition phases independently programmable
- Ignition voltage control
- Transition mode PFC with over-current protection
- Programmable and precise End-of-life protection compliant with all ballast configurations
- Auto-adjusting half-bridge over-current control
- Automatic re-lamp
- 3% oscillator precision
- 1.2μs dead time
- PFC over-voltage protection and feedback disconnection
- Under voltage lock-out



Applications

- Electronic ballast

Figure 1. Block diagram



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1 Device description

Designed in High-voltage BCD Off-line technology, the L6585D embeds a PFC controller, a half-bridge controller, the relevant drivers and the logic necessary to build an electronic ballast.

The advanced and precise logic circuitry, combined with the programmability of the End-of-Life windows comparator threshold, makes the L6585D compliant with either "lamp-to-ground" or "block capacitor-to ground" configurations.

Another outstanding feature is the possibility of controlling and limiting the lamp voltage during the ignition phase.

The pre-heating and ignition durations are independently settable as well as the half-bridge switching frequencies for each operating phases (pre-heating, ignition and normal mode).

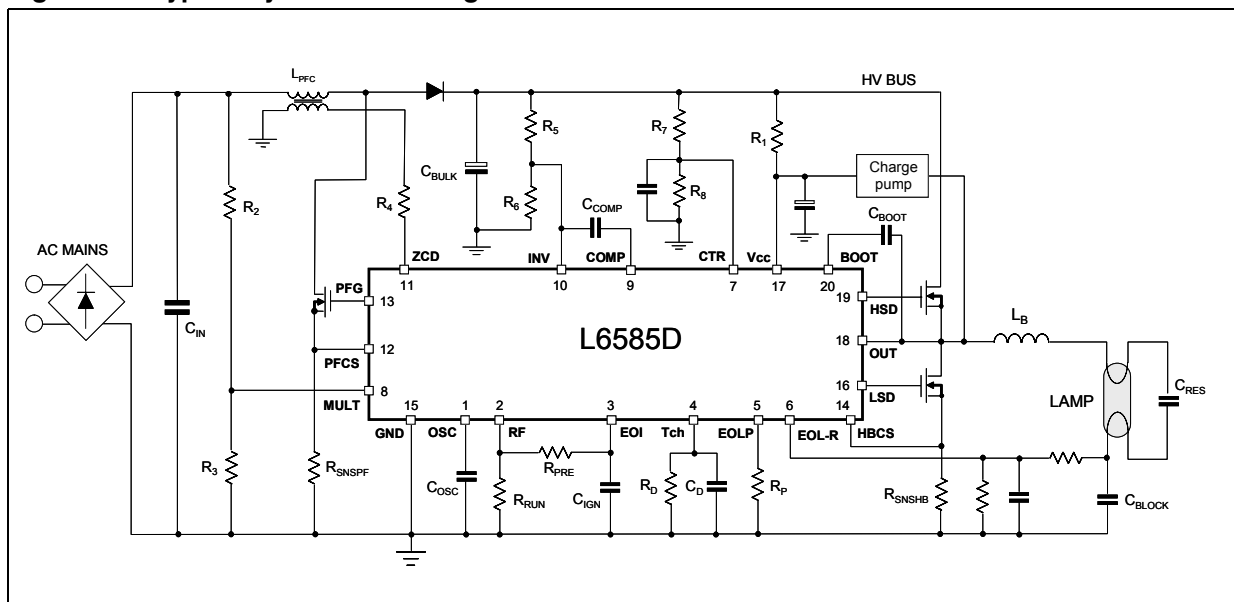
Other features (half-bridge over-current with frequency increase, PFC over-voltage) allow building a reliable and flexible solution with a reduced part count.

The PFC section achieves current mode control operating in Transition Mode; the highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The PFC output voltage is controlled by means of a voltage-mode error amplifier and a precise internal voltage reference.

The driver of the PFC is able to provide 300mA (source) and 600mA (sink) and the drivers of the half-bridge provide 290mA source and 480mA sink.

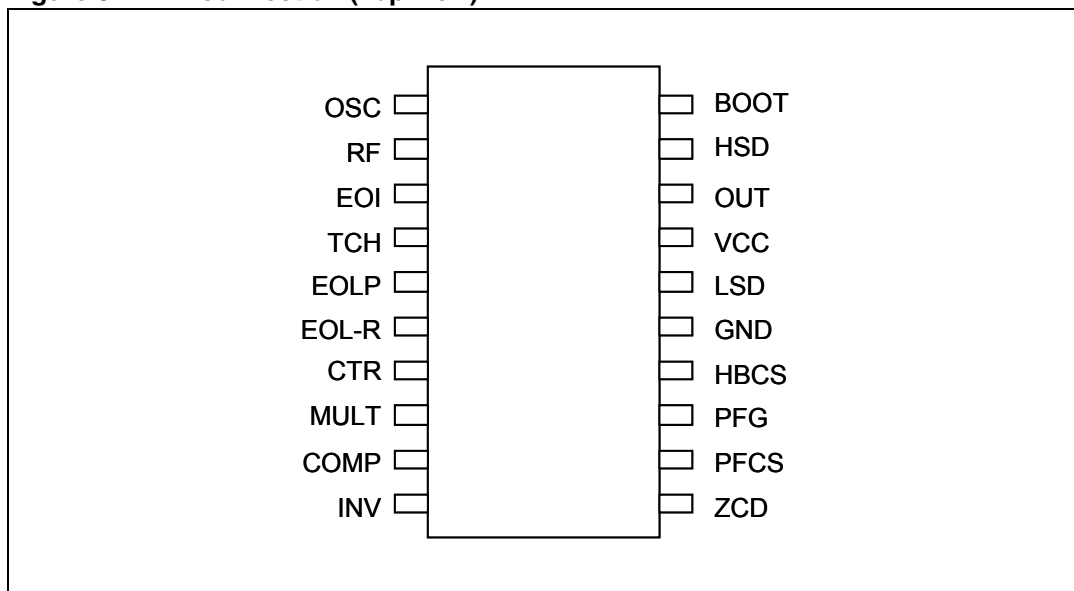
Figure 2. Typical system block diagram



2 Pin settings

2.1 Connection

Figure 3. Pin sonnection (Top view)



2.2 Functions

Table 1. Pin functions

| Pin num. | Name | Function |
|----------|-------|---|
| 1 | OSC | An external capacitor to GND fixes the half-bridge switching frequency with a $\pm 3\%$ precision. |
| 2 | RF | Voltage reference able to source up to $240\mu\text{A}$; the current sunk from this pin fixes the switching frequency of the half-bridge for each operating state. A resistor (R_{RUN}) connected to ground sets the half-bridge operating frequency combined with the capacitor connected to the pin OSC. A resistor connected to EOI (R_{PRE}) – in parallel with R_{RUN} – sets the maximum half-bridge switching frequency during pre-heating. |
| 3 | EOI | Connected to ground by a capacitor that, combined with R_{PRE} , determines the ignition duration Pre-heating: low impedance to set high switching frequency Ignition and run mode: high impedance with controlled current sink in case of HBCS threshold triggering. |
| 4 | Tch | Pin for setting the pre-heating time and the protection intervention. Connect a RC parallel network (R_{D} and C_{D}) to ground Pre-heating: the C_{D} is charged by an internal current generator. When the pin voltage reaches 4.63V the generator is disabled and the capacitor discharges because of R_{D} ; once the voltage drops below 1.52V, the preheating finishes, the ignition phase starts and the $R_{\text{D}}C_{\text{D}}$ is discharged to ground. Run mode: according to the kind of fault (either over-current or EOL) the internal generator charges the RC parallel network and appropriate actions are taken to stop the application. During proper behavior of the IC, this pin is low impedance. |
| 5 | EOLP | Pin to program the EOL comparator. It is possible to select both the EOL sensing method and the window comparator amplitude by connecting a resistor (R_{EOLP}) to ground. |
| 6 | EOL-R | Input for the window comparator and re-lamp function. It can be used to detect the lamp ageing for either “lamp to ground” and “block capacitor to ground” configurations. According to the EOLP pin setting, it is possible to program: – the window amplitude (V_{W}) – the center of the window (V_{SET}) either fixed or in tracking with the PFC output bus. This function is blanked during the ignition phase. In case of either lamp disconnection or removal, a second threshold ($V_{\text{SL-UP}}$) crossing latches the IC and drives the chip in “ready-mode” so that when the voltage at EOL-R pin is brought below $V_{\text{SL-DOWN}}$ (re-lamp) a new pre-heating/ignition sequence is repeated. |
| 7 | CTR | Input pin for: – PFC over-voltage detection: the PFC driver is stopped until the voltage returns in the proper operating range – Feedback disconnection detection – reference for End-of-life in case tracking reference; – shut-down: forcing the pin to a voltage lower than 0.75V, the IC shuts down in unlatched condition. |
| 8 | MULT | Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the PFC current loop. |

Table 1. Pin functions (continued)

| Pin num. | Name | Function |
|----------|-------|--|
| 9 | COMP | Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the PFC voltage control loop and ensure high power factor and low THD. |
| 10 | INV | Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. Input for the feedback disconnection comparator |
| 11 | ZCD | Boost inductor's demagnetization sensing input for PFC transition-mode operation. A negative-going edge triggers PFC MOSFET turn-on. During start-up or when the voltage is not high enough to arm the internal comparator (e.g. AC Mains peak), the PFC driver is triggered by means of an internal starter. |
| 12 | PFC S | Input to the PFC PWM comparator. The current flowing in the PFC mosfet is sensed by a resistor; the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine the PFC MOSFET' s turn-off. A second comparison level detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, shuts down and latches the IC reducing its consumption to the start-up. An internal LEB prevents undesired function triggering. |
| 13 | PFG | PFC gate driver output. The totem pole output stage is able to drive power MOSFET'S with a peak current of 300mA source and 600mA sink. |
| 14 | HBCS | 2-levels half-bridge current monitor for current control. The current flowing in the HB mosfet is sensed by a resistor; the resulting voltage is applied to this pin. Low threshold (active during run mode): in case of thresholds crossing, the IC reacts with self-adjusting frequency increase in order to limit the half-bridge (lamp) current. High threshold: – ignition: in case of thresholds crossing during the frequency shift, the IC reacts with self-adjusting frequency increase in order to limit the lamp voltage and preventing operation below resonance. – run mode: in case of thresholds crossing because of current spikes (due e. g. to capacitive mode / cross-conduction), the L6585D latches to avoid MOSFETs damaging, |
| 15 | GND | Ground. Current return for both the signal part of the IC and the gate driver. |
| 16 | LSD | Low side driver output: the output stage can deliver 290mA source and 480mA sink (typ. values). |
| 17 | VCC | Supply Voltage of both the signal part of the IC and the gate driver. Clamped with a Zener inside. |
| 18 | OUT | High Side Driver Floating Reference. This pin must be connected close to the source of the high side power MOS. |
| 19 | HSD | High side driver output: the output stage can deliver 290mA source and 480mA (typ. values). |
| 20 | BOOT | Bootstrapped Supply Voltage. Between this pin and V _{CC} , the bootstrap capacitor must be connected. A patented integrated circuitry replaces the external bootstrap diode, by means of a high voltage DMOS, synchronously driven with the low side power MOSFET. |

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Pin | Parameter | Value | Unit |
|-----------------------|--------------------------|---|------------------------------|------|
| V _{BOOT} | 20 | Floating supply voltage | -1 to 618 | V |
| V _{OUT} | 18 | Floating ground voltage | -3 to V _{BOOT} - 18 | V |
| dV _{OUT} /dt | 18 | Floating ground max. slew rate | 50 | V/ns |
| V _{CC} | 17 | IC Supply voltage (I _{CC} = 20mA) ⁽¹⁾ | Self-limited | V |
| | 1, 3, 4, 8, 10, 12 | Analog input and outputs | -0.3 to 5 | V |
| | 2, 5 | | -0.3 to 2.7 | V |
| | 6 | | V _{cc} | |
| | 7 | | -0.3 to 7 | V |
| | 14 | | -5 to 5 | |
| | 9, 11 | ZCD clamp (I _{ZCD} < 4mA) | Self-limited | |
| I _{RF} | 2 | Current capability | 240 | μA |
| I _{EOLP} | 5 | Current capability | 100 | μA |
| F _{OSC(MAX)} | | Maximum operating frequency | 250 | KHz |
| P _{TOT} | | Power dissipation @T _A = 70°C | 0.83 | W |

1. The device has an internal Clamping Zener between GND and the VCC pin, it must not be supplied by a Low Impedance Voltage Source.

Note: ESD immunity for pins 18, 19 and 20 is guaranteed up to 900V (Human Body Model)

3.2 Thermal data

Table 3. Thermal data

| Symbol | Description | Value | Unit |
|-------------------|---|------------|------|
| R _{thJA} | Max. thermal resistance junction to ambient | 120 | °C/W |
| T _J | Junction operating temperature range | -40 to 150 | °C |
| T _{STG} | Storage temperature | -55 to 150 | °C |

4 Electrical characteristics

$V_{CC} = 15V$, $T_A = 25^\circ C$, $C_L = 1nF$, $C_{OSC} = 470pF$, $R_{RUN} = 47K$, unless otherwise specified

Table 4. Electrical characteristics

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|-----------------|----------------------------------|---|--------|------|------|------|
| Supply voltage | | | | | | | |
| V _{CC} | V _{CC} | Operating range | After turn-on | 11 | | 16 | V |
| V _{CC(on)} | V _{CC} | Turn-on threshold | (1) | 13.6 | 14.3 | 15 | V |
| V _{CC(OFF)} | V _{CC} | Turn-off threshold | (1) | 9.6 | 10.3 | 11 | V |
| VZ | V _{CC} | Zener Voltage | I _{CC} = 20mA | 16.2 | 17.2 | 17.7 | V |
| Supply current | | | | | | | |
| I _{ST-UP} | V _{CC} | Start-up current | Before turn-on @ 13V | | 250 | 370 | μA |
| I _{CC} | V _{CC} | Operating supply current | | | 7 | | mA |
| I _q | V _{CC} | Residual current | IC latched | | | 370 | μA |
| PFC section – multiplier input | | | | | | | |
| I _{MULT} | MULT | Input bias current | V _{MULT} = 0 | | | -1 | μA |
| V _{MULT} | MULT | Linear operation range | V _{COMP} = 3V | 0 to 3 | | | V |
| $\frac{\Delta V_{CS}}{\Delta V_{MULT}}$ | MULT | Output max. slope | V _{MULT} = 0 to 1V, V _{COMP} = Upper clamp | | 0.75 | | V/V |
| K _M | MULT | Gain | V _{MULT} = 1V, V _{COMP} = 3V | | 0.52 | | 1/V |
| PFC section – error amplifier | | | | | | | |
| V _{INV} | INV | Voltage feedback input threshold | | 2.45 | 2.5 | 2.55 | V |
| | INV | Line regulation | V _{CC} = 10.3V to 16V | | | 50 | mV |
| I _{INV} | INV | Input bias current | | | | -1 | μA |
| G _v | INV | Voltage gain | Open loop (2) | 60 | 80 | | dB |
| GB | INV | Gain-bandwidth product | (2) | | 1 | | MHz |
| I _{COMP} | COMP | Source current | V _{COMP} = 4V, V _{INV} = 2.4 V | | -2.6 | | mA |
| | | Sink current | V _{COMP} = 4V, V _{INV} = 2.6 V | | 4 | | mA |
| V _{COMP} | COMP | Upper clamp voltage | I _{SOURCE} = 0.5 mA | | 4.2 | | V |
| | | Lower clamp voltage | I _{SINK} = 0.5 mA | | 2.25 | | V |
| V _{DIS} | INV | Open loop detection threshold | CTR > 3.4 | | 1.2 | | V |
| | COMP | Static OVP threshold | | 2.1 | 2.25 | 2.4 | V |

Table 4. Electrical characteristics (continued)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|------|--|---|------|------|------|---------------|
| CTR pin | | | | | | | |
| DIS | CTR | Disable threshold | Falling edge | | 0.75 | | V |
| | | Hysteresys | | | 120 | | mV |
| PFOV | CTR | Dynamic PFC overvoltage | Rising edge | | 3.4 | | V |
| | | Hysteresys | | | 140 | | mV |
| | CTR | Available range as tracking reference | Lower threshold (falling) | | 1.7 | | V |
| | | | Hysteresys | | 0.12 | | |
| | | | Higher threshold (rising) | | 3.4 | | V |
| | | | Hysteresys | | 0.14 | | |
| PFC section – current sense comparator | | | | | | | |
| ICS | PFCS | Input bias current | $V_{CS} = 0$ | | | -1 | μA |
| tLEB | PFCS | Leading edge blanking | (2) | 100 | 200 | 300 | ns |
| VCSdis | PFCS | IC disable level | | 1.65 | 1.75 | 1.85 | V |
| td(H-L) | PFCS | Delay to output | | | 120 | | ns |
| $V_{CSclamp}$ | PFCS | Current sense reference clamp | $V_{COMP} = \text{Upper clamp}$ | 1.0 | 1.08 | 1.16 | V |
| PFC section – zero current detector | | | | | | | |
| VZCDH | ZCD | Upper clamp voltage | $I_{ZCD} = 2.5 \text{ mA}$ | 5 | | | V |
| VZCDL | ZCD | Lower clamp voltage | $I_{ZCD} = -2.5 \text{ mA}$ | -0.3 | 0 | 0.3 | V |
| VZCDA | ZCD | Arming voltage (positive-going edge) | (2) | | 1.4 | | V |
| VZCDT | ZCD | Triggering voltage (negative-going edge) | (2) | | 0.7 | | V |
| I_ZCDb | ZCD | Input bias current | $V_{ZCD} = 1 \text{ to } 4.5 \text{ V}$ | | | 1 | μA |
| I_{ZCDsrc} | ZCD | Source current capability | | -4 | | | mA |
| I_{ZCDsnk} | ZCD | Sink current capability | | 4 | | | mA |
| PFC section – gate driver | | | | | | | |
| | PFG | Output high/low | $I_{SINK} = 10\text{mA}$ | | | 0.2 | V |
| | | | $I_{SOURCE} = 10\text{mA}$ | 14.5 | | | V |
| t _f | PFG | Fall time | | | 40 | 90 | ns |
| t _r | PFG | Rise time | | | 90 | 140 | ns |
| I_{SINK} | PFG | Peak sink current | | 475 | 600 | | mA |
| I_{SOURCE} | PFG | Peak source current | | 200 | 300 | | mA |
| | PFG | Pull-down resistor | | | 10 | | k Ω |

Table 4. Electrical characteristics (continued)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|--|----------|--|--|-------------------|-------|-------|----------|
| Half bridge section – Timing & oscillator | | | | | | | |
| I_{CH} | T_{CH} | Charge current | $V_{TCH} = 2.2V$ | | 30 | | μA |
| V_{CHP} | T_{CH} | Charge threshold (positive going-edge) | (1) | | 4.63 | | V |
| V_{CHN} | T_{CH} | Discharge threshold (negative going edge) | (1) | | 1.50 | | V |
| | T_{CH} | Leakage current | $1.5V < V_{TCH} < 4.5V$, falling | | | 0.1 | μA |
| R_{TCH} | T_{CH} | Internal impedance | Run mode | | 150 | 200 | Ω |
| | EOI | Open state current | $V_{EOI} = 2V$ | | | 0.15 | μA |
| R_{EOI} | EOI | EOI impedance | During pre-heating | | | 150 | Ω |
| I_{EOI} | EOI | EOI current generator during ignition and run mode | $T_{spike} = 200ns^{(3)}$ | | 20 | | μA |
| | | | $T_{spike} = 400ns^{(3)}$ | | 100 | | |
| | | | $T_{spike} = 600ns^{(3)}$ | | 200 | | |
| | | | $T_{spike} = 1\mu s^{(3)}$ | | 270 | | |
| V_{EOI} | EOI | EOI threshold | (1) | 1.83 | 1.9 | 1.98 | V |
| V_{REF} | RF | Reference voltage | (1) | 1.92 | 2 | 2.08 | V |
| IRF | RF | Max current capability | | 240 | | | μA |
| | OSC | Rising threshold | (1) | | 3.7 | | V |
| | OSC | Falling threshold | (1) | | 0.9 | | V |
| D | OSC | Output duty cycle | | 48 | 50 | 52 | % |
| T_{DEAD} | OSC | Dead time | | 0.96 | 1.2 | 1.44 | μs |
| f_{RUN} | OSC | Half-bridge oscillation frequency (run mode) | | 58.4 | 60.2 | 62 | KHz |
| f_{PRE} | OSC | Half-bridge oscillation frequency (pre heating) | $R_{PRE}=50K$ | 113.2 | 116.7 | 120.2 | KHz |
| Half bridge section – End Of Life FUNCTION and re-lamp comparator | | | | | | | |
| | EOLP | Current capability | | 100 | | | μA |
| | EOLP | Reference voltage | | 1.92 | 2 | 2.08 | V |
| | EOL-R | Operating range | $EOLP=27K$ | 0.95 | | 4.15 | V |
| V_S | EOL-R | Window comparator reference | $220K = R_{EOLP} = 270K$ or $22K = R_{EOLP} = 27K$ | tracking with CTR | | | V |
| | | | $R_{EOLP} > 620K$ or $75K = R_{EOLP} = 91K$ | | 2.5 | | |
| V_W | | Half window amplitude | $220K = R_{EOLP} = 270K$ or $75K = R_{EOLP} = 91K$ | | 220 | | mV |
| | | | $R_{EOLP} > 620K$ or $22K = R_{EOLP} = 27K$ | | 720 | | mV |

Table 4. Electrical characteristics (continued)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|-------|---|---|------|-----------------------|----------------------|------------------|
| | EOL-R | Sink/source capability | | | 2.5 | | μA |
| | EOL-R | Relamp comparator | | | 4.63 | | V |
| | | hysteresys | | | 160 | | mV |
| Half bridge section – Half-bridge current sense | | | | | | | |
| HBCSH | HBCS | Frequency increase threshold | $V_{EOI} < 1.9\text{V}$ (<i>ignition</i>) | 1.53 | 1.6 | 1.66 | V |
| HBCSL | HBCS | | $V_{EOI} > 1.9\text{V}$ (<i>run mode</i>) | 0.85 | 0.91 | 0.97 | V |
| | HBCS | Latched threshold | <i>Run mode</i> | 1.53 | 1.6 | 1.66 | V |
| Half bridge section – Low side gate driver | | | | | | | |
| | LSD | Output low voltage | $I_{\text{SINK}} = 10\text{mA}$ | | | 0.3 | V |
| | LSD | Output high voltage | $I_{\text{SOURCE}} = 10\text{mA}$ | 14.5 | | | V |
| | LSD | Peak source current | | 200 | 290 | | mA |
| | LSD | Peak sink current | | 400 | 480 | | mA |
| T_{RISE} | LSD | Rise time | | | 120 | | ns |
| T_{FALL} | LSD | Fall time | | | 80 | | ns |
| | LSD | Pull-down resistor | | | ; | 45 | $\text{K}\Omega$ |
| Half bridge section – High side gate driver (voltages referred to OUT) | | | | | | | |
| | HSD | Output low voltage | $I_{\text{SINK}} = 10\text{mA}$ | | | $V_{\text{OUT}+0.3}$ | V |
| | HSD | Output high voltage | $I_{\text{SOURCE}} = 10\text{mA}$ | | $V_{\text{BOOT}-0.5}$ | | V |
| | HSD | Peak source current | | 200 | 290 | | mA |
| | HSD | Peak sink current | | 400 | 480 | | mA |
| T_{RISE} | HSD | Rise time | | | 120 | | ns |
| T_{FALL} | HSD | Fall time | | | 80 | | ns |
| | HSD | HSD-OUT pull-down | | | 50 | | $\text{K}\Omega$ |
| High-side floating gate-drive supply | | | | | | | |
| | BOOT | Leakage current | $V_{\text{BOOT}} = 600\text{V}^{(2)}$ | | | 5 | μA |
| | OUT | Leakage current | $V_{\text{OUT}} = 600\text{V}^{(2)}$ | | | 5 | μA |
| | | Synchronous bootstrap diode on-resistance | $V_{\text{LSD}} = \text{HIGH}$ | | 250 | | Ω |

- Parameter in tracking
- Specification over the -40°C to 125°C junction temperature range are ensured by design, characterization and statistical correlation
- A pulse train has been sent to the HBCS pin with $f=6\text{KHz}$; the pulse duration is the one indicated in the notes as "TON"

5 Application information

5.1 Start-up sequence

5.1.1 Pre-heating (time interval A *Figure 5*)

After IC turn-on, unless a lamp absence is detected, the oscillator starts switching at a frequency (f_{PRE}) set by values of C_{OSC} and R_{RUN} and R_{PRE} *Figure 4*:

Equation 1

$$f_{PRE} = \frac{1.328}{C_{OSC} \cdot (R_{RUN} \parallel R_{PRE})}$$

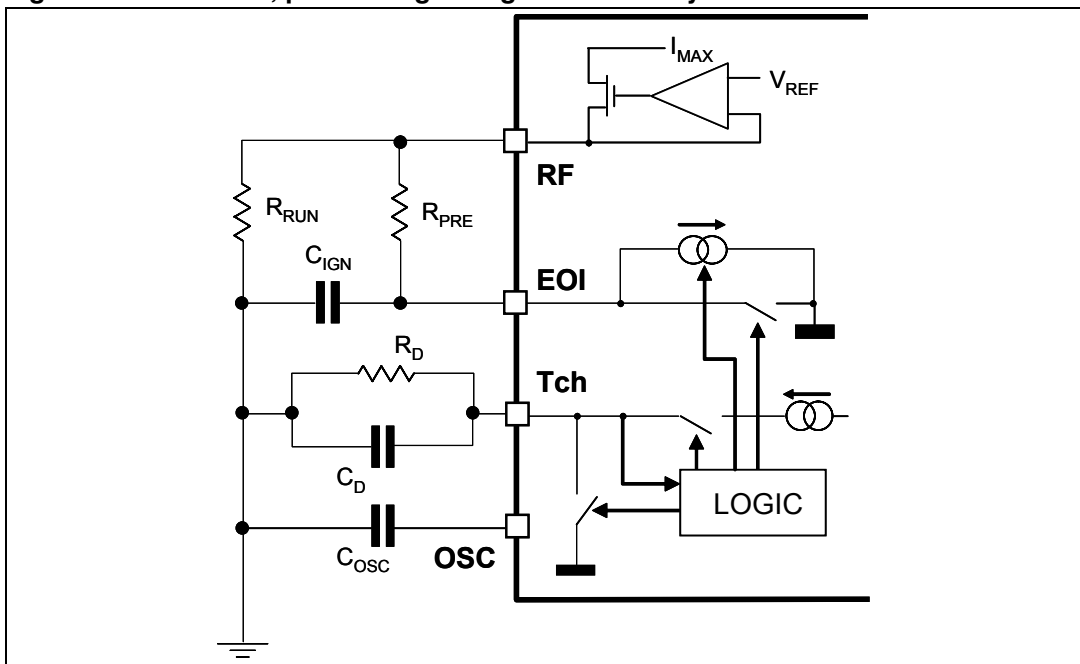
The *pre-heating time* is:

Equation 2

$$T_{PRE} = 4.63 \cdot \frac{C_D}{I_{CH}} + R_D \cdot C_D \cdot \ln \frac{4.63}{1.52}$$

where C_D and R_D are shown in *Figure 4* and I_{CH} is typically 34 μ A.

Figure 4. Oscillator, pre-heating and ignition circuitry



5.1.2 Ignition (time interval B [Figure 5](#))

When the voltage at pin T_{CH} drops down to 1.50V (typ.), the pin EOI is driven in high impedance state and C_{IGN} is exponentially charged according to the time constant τ given by C_{IGN}·R_{PRE} that defines the *ignition time* and the frequency shift starts.

The *ignition time* is the time necessary to EOI voltage to reach 1.9V, so, by means of simple calculation:

Equation 3

$$T_{IGN} = 3 \cdot C_{IGN} \cdot R_{PRE}$$

During this phase, the half-bridge current control can **limit the maximum voltage applied to the lamp** by forcing small frequency increases whenever the half-bridge sense resistor voltage exceeds the HBCSH threshold (see the “Half-Bridge current control” paragraph).

[Figure 5](#), centre and right, shows the L6585D behavior as the lamp gets older; if it doesn't ignite for a time longer than the pre-heating one (counted by a cycle charge/discharge of the T_{CH} pin), the IC is stopped, enters low consumption and waits for either a re-lamp or an UVLO.

5.1.3 Run mode (time interval C *Figure 5*)

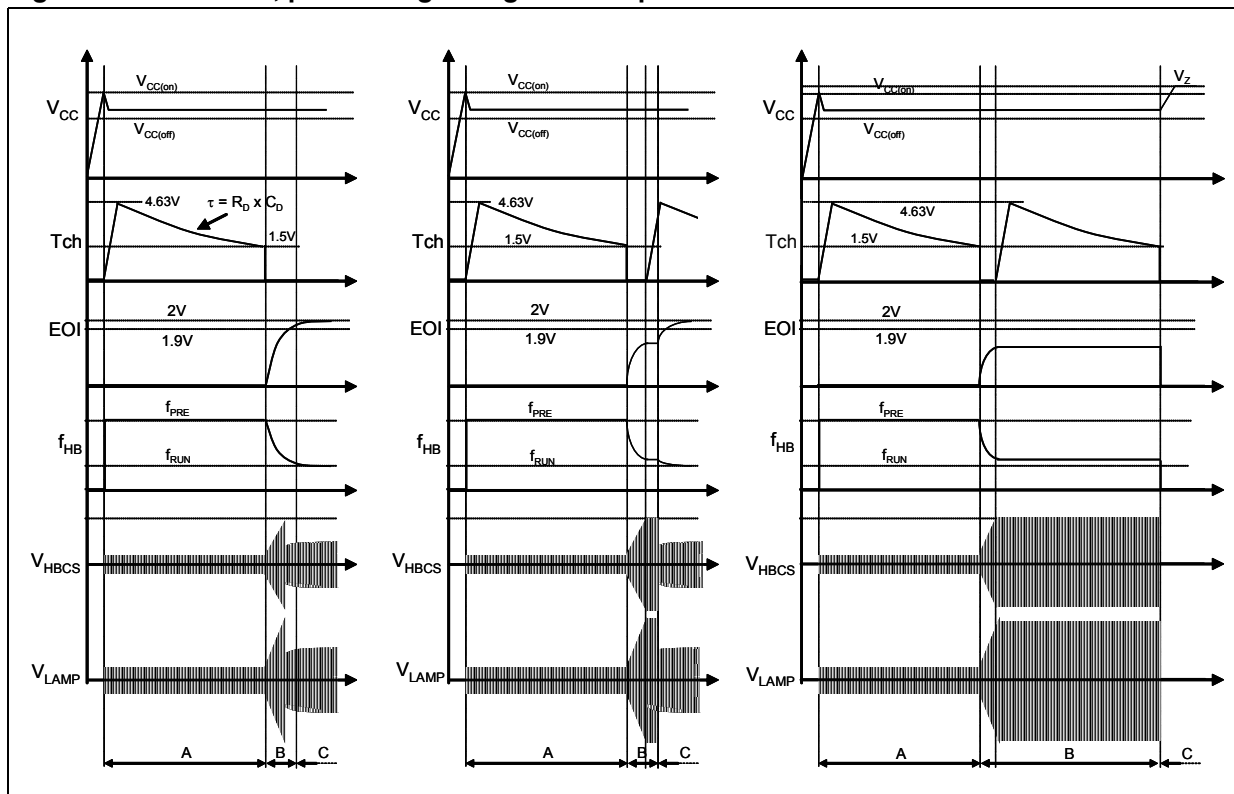
As the voltage at EOI exceeds 1.9V and the lamp has ignited, the L6585D enters *Run mode* and remains in this condition unless one of the protections (all enabled in this mode) is triggered.

The switching frequency reaches the f_{RUN} value set by R_{RUN} and C_{OSC} :

Equation 4

$$f_{RUN} = \frac{1.328}{R_{RUN} \cdot C_{OSC}}$$

Figure 5. Oscillator, pre-heating and ignition sequence



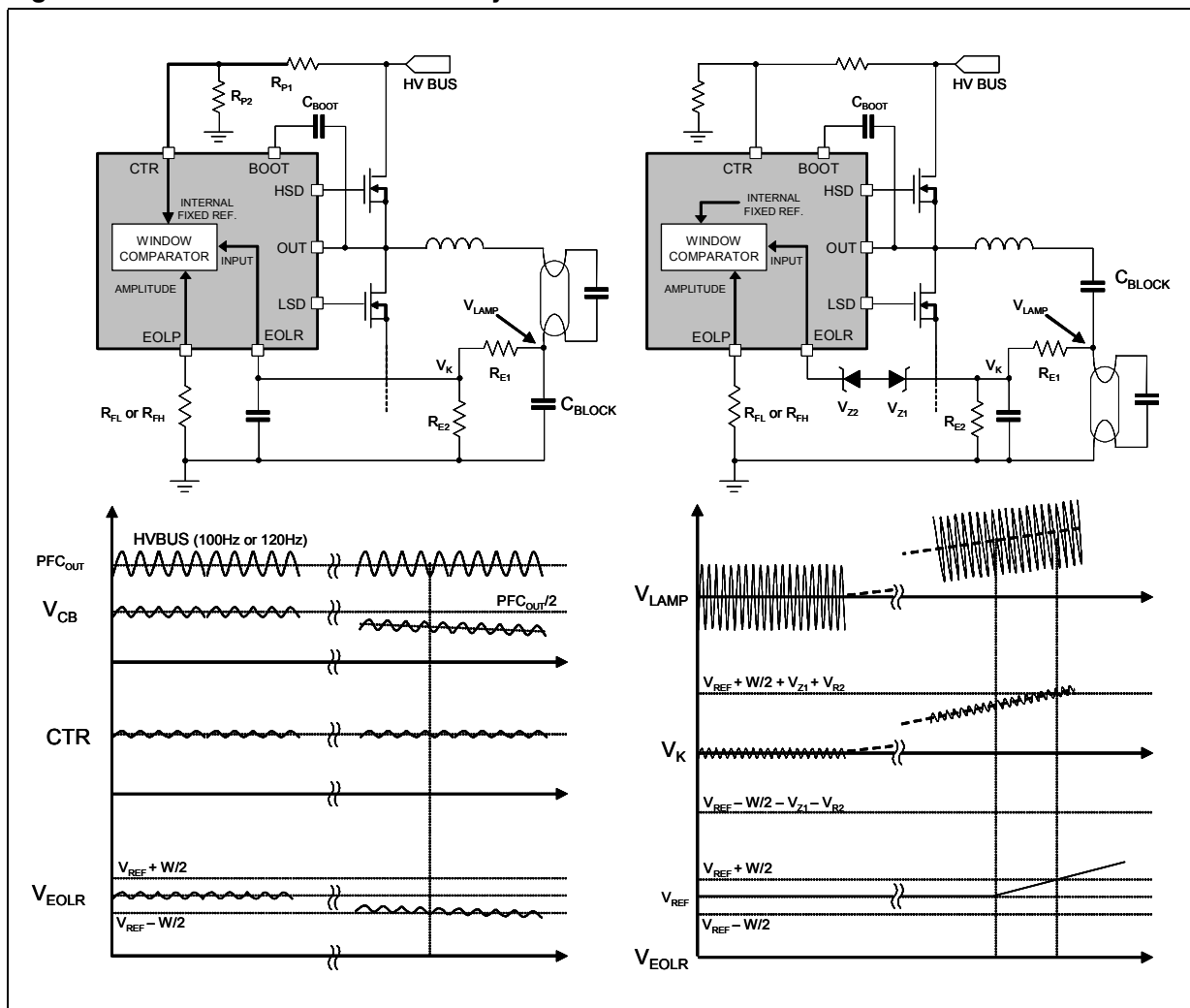
6 End of life – window comparator

To detect the ageing of the lamp with particular attention to the effect appearing as asymmetric rectification, a *programmable* window comparator has been introduced (centered around “ V_{REF} ” with amplitude “ V_W ”) that triggers when the EOL-R voltage is higher than $V_{REF} + V_W/2$ or lower than $V_{REF} - V_W/2$.

By means of the resistor connected to the EOLP pin, it is possible to select:

1. the **sensing mode**:
 - **fixed reference**: the centre of the window comparator (V_{REF}) is fixed at 2.5V by an internal reference;
 - **tracking reference**: the centre of the window comparator is the voltage at pin CTR (that is a signal proportional to the PFC output voltage).
2. the half-window amplitude ($V_W/2$): 220mV or 720mV.

Figure 6. End-of-life detection circuitry and waveforms



The four possible configurations are summarized in the following table, together with the value of resistance to be connected to the EOLP pin in order to obtain the desired setting:

Table 5. Configuration of the EOLP pin

| EOLP resistor | Symbol | Reference | Half-window amplitude |
|--------------------------|----------|-------------------|-----------------------|
| $R_{EOLP} > 620K$ | R_{FH} | Fixed 2.5V | $\pm 720mV$ |
| $220K = R_{EOLP} = 270K$ | R_{TL} | Tracking with CTR | $\pm 220mV$ |
| $75K = R_{EOLP} = 91K$ | R_{FL} | Fixed 2.5V | $\pm 220mV$ |
| $22K = R_{EOLP} = 27K$ | R_{TL} | Tracking with CTR | $\pm 720mV$ |

Tracking reference: this setting is suitable for the block capacitor to ground configuration ([Figure 6](#), left).

In this case the window comparator centre is set by the CTR voltage that is internally transferred to the EOL structure.

The effect of rectification appears as shifting of the DC voltage component across the block capacitor, which, under normal conditions, equals one half of the PFC output voltage.

A signal proportional to the DC block capacitor voltage is sent to the EOL-R pin by means of a resistive divider (R_{E1} and R_{E2}); the dividers R_{E1} and R_{E2} and R_{P1} and R_{P2} must be designed to set the EOL-R voltage equal to CTR under nominal condition.

Fixed reference: this setting is suitable for the lamp to ground configuration ([Figure 6](#), right).

The effect of rectification appears as shifting of the DC lamp voltage.

A resistive divider (R_{E1} and R_{E2}) senses the voltage across the lamp under normal condition, that is an AC signal with zero average value whereas in case of asymmetric rectification the DC value can shift either in positive or negative direction. Two Zener diodes can be connected back-to-back between the EOL-R pin and the centre of the resistive divider.

The Zener voltages should differ by an amount as close as possible to the double of the internal reference to have a symmetrical detection, as it can easily be obtained from the following equations:

- $V_{UP} = V_{REF} + W/2 + V_{Z1} + V_{R2}$
- $V_{DOWN} = V_{REF} - W/2 - V_{Z2} - V_{R1}$

where V_{UP} and V_{DOWN} are the V_K values (equal in absolute value) that trigger the window comparator.

To avoid an immediate intervention of the EOL protection, a filtering is introduced; as long as the fault condition persists, the Tch internal generator charges the C_D up to 4.63V and then it opens. If this fault condition is still present when the Tch voltage decreases down to 1.5V, then the half bridge is stopped, otherwise (if the fault disappears) the counting is stopped and reset.

7 Half-bridge current control

The information about the lamp current can be obtained by reading the voltage across a sense resistor placed in series to the source of the half-bridge low side MOS.

This circuitry is enabled at the end of the pre-heating phase and it enriches the L6585D with two features:

- **Controlled lamp voltage/current** during *ignition* ([Figure 5](#)): by properly setting the sense resistor (such that the V_{HBCS} level is crossed in correspondence of a lamp voltage higher than the ignition voltage) it is possible to limit the maximum lamp voltage during ignition. In case of this occurrence, then the L6585D would react with a small frequency increase that allows limiting the lamp voltage (V_{+IGN}). This also prevents the risk of crossing the resonance frequency of the $L_{BALLAST}C_{RES}$ circuit. If the lamp ignites before T_{CH} reaches 1.50V ([Figure 5](#) left) that is EOI has exceeded 1.9V, then:
 - EOI internal switch opens and its voltage moves asymptotically to 2V
 - The switching frequency reaches the operating one;
 - When T_{CH} reaches 1.52, it will be discharged

If instead that the lamp hasn't ignited after a time equal to the pre-heat time ([Figure 5](#) right) the oscillator stops, the chip enters low consumption mode and this condition is latched until the mains supply voltage is removed or a re-lamp is detected.

- **Over-current protection** during *run mode*: if the HBCSL threshold is crossed, the T_{CH} internal generator is turned on as well as the one at pin EOI causing a frequency increase: this implements a **current control** structure.

During *run mode* another protection is active: a second comparator (HBCSH) on the pin HBCS detects anomalous current flow through the sense resistor such as the spikes generated by the **capacitive mode**; the crossing of this second threshold latches the IC.

8 CTR

This is a multi-function pin, connected to a resistive divider to the PFC output bus:

- **PFC over-voltage:** in case of PFC output overshoot (e.g. at start-up) that causes a threshold crossing, the PFC section stops switching until the pin voltage falls below 3.26V (typ.); this is helpful because the bandwidth of the PFC error amplifier is narrow so the control loop is not fast enough to properly react
- **Feedback disconnection:** The OVP function above described (together with the static one embedded in the PFC error amplifier) is able to handle “normal” over-voltage conditions, i.e. those resulting from an abrupt load/line change or occurring at start-up. In case of over-voltage generated when the upper resistor of the feedback output divider fails open, the control loop can no longer read the information on the output voltage and will force the PFC pre-regulator to work at maximum ON time; if this occurs (i.e. the pin INV falls below 1.2V, typ.) and the CTR detects an OVP, the gate drivers activity is immediately stopped, the device enters low consumption and the condition is latched as long as the IC supply voltage is above the UVLO threshold;
- **Reference** for EOL in case of tracking reading.
- **Disable:** by forcing the pin below 0.75V an immediate unlatched shut-down is activated; it can be also used as **re-lamp** in fact after the pin voltage is above 0.8V a pre-heating/ignition sequence is repeated.

9 Re-lamp

A second comparator has been introduced on the pin EOL-R; a voltage higher than the internal threshold is read as **lamp absence** so the chip suddenly stops switching, enters idle mode (low consumption) and is ready for a new pre-heating/ignition sequence as soon as a new lamp is inserted.

In this idle mode the consumption of the chip is reduced so that the current flowing through the resistors (connected to the high voltage bus for the start-up) is enough to keep the V_{CC} voltage above the UVLO threshold.

After a re-lamp cycle (that is the EOL-R voltage is brought above 4.63V and then released below), a new pre-heating/ignition sequence starts.

Table 6. IC configuration

| | Pre-heating | Ignition | Run mode |
|---------------------------------|---|---|--|
| Time duration | T_{CH} cycle ⁽¹⁾ ; It depends on R_D and C_D | EOI charge from 0 to 1.9V (typ.); It depends on R_D and C_D | Until a fault appears or the AC Mains is removed |
| Half-bridge switching frequency | $f_{PRE} = \frac{1.328}{C_{OSC} \cdot (R_{RUN} \parallel R_{PRE})}$ | The frequency shifts from f_{PRE} to f_{RUN} with exponential trend | $f_{RUN} = \frac{1.328}{R_{RUN} \cdot C_{OSC}}$ |
| RELAMP comparator | ENABLED | ENABLED | ENABLED |
| CTR: PFC overvoltage | ENABLED | ENABLED | ENABLED |
| CTR: disable function | ENABLED | ENABLED | ENABLED |
| Half-bridge current sense | DISABLED | ENABLED – low threshold \Rightarrow disabled – high threshold \Rightarrow F_{SW} increase | ENABLED – low threshold \Rightarrow F_{SW} increase – high threshold \Rightarrow latch |
| EOL: window comparator | DISABLED | DISABLED | ENABLED |
| PFC choke saturation | ENABLED | ENABLED | ENABLED |

1. T_{CH} cycle: charge of the T_{CH} voltage up to 4.63V and discharge down to 1.50V following the $R_D C_D$ time constant

Table 7. Fault conditions

| Fault | Condition | IC behavior | Action required |
|---|---|---|--|
| Lamp absence (re-lamp comparator) | <i>At turn-on:</i> EOL-R voltage higher than 4.63V | <ul style="list-style-type: none"> – The T_{CH} charge doesn't start (no ignition) – Drivers stopped – IC low consumption (V_{CC} clamped) | Lamp replacement (EOL-R below 4.63V) |
| | <i>Run mode:</i> EOL-R voltage higher than 4.63V | <ul style="list-style-type: none"> – All drivers stopped – IC low consumption (V_{CC} clamped) | |
| End of life | EOL-R voltage outside the limits of window comparator | <ul style="list-style-type: none"> – T_{CH} cycle ⁽¹⁾ (reset if the fault disappears) – drivers stopped at the end of T_{CH} cycle – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾ |
| Half-bridge current sense | <i>Ignition:</i> HBCS threshold | <ul style="list-style-type: none"> – T_{CH} cycle ⁽¹⁾ with lamp voltage control – In case of HBCS at the end of the T_{CH} cycle, drivers stopped – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾ |
| | <i>Run mode:</i> HBCSL threshold | <ul style="list-style-type: none"> – T_{CH} cycle ⁽¹⁾ with lamp voltage control (frequency increase) – In case of HBCS at the end of the T_{CH} cycle, drivers stopped – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾ |
| | <i>Run mode:</i> HBCSH threshold | <ul style="list-style-type: none"> – Drivers stopped – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾ |
| Shut-down | CTR voltage lower than 0.8V | <ul style="list-style-type: none"> – Drivers stopped – IC low consumption (V_{CC} clamped) | When the CTR voltage returns above 0.8V, the IC driver restart with a pre-heating sequence |
| Choke saturation | PFCS voltage higher than 1.6V | <ul style="list-style-type: none"> – Drivers stopped – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾⁽³⁾ |
| Over-voltage of PFC output | CTR voltage higher than 3.4V | <ul style="list-style-type: none"> – PFC driver stopped | When the CTR voltage returns below 3.26V (Typ.), the PFC driver restarts |
| PFC open loop (feedback disconnection) | CTR voltage higher than 3.4V AND INV voltage lower than 1.2 | <ul style="list-style-type: none"> – Drivers stopped – IC low consumption (V_{CC} clamped) | Re-lamp cycle ⁽²⁾⁽³⁾ |

1. T_{CH} cycle: charge of the T_{CH} voltage up to 4.63V and discharge down to 1.50V following the R_{DCD} time constant;
2. Re-lamp cycle: the voltage at EOL-R pin must be first pulled above 4.63V and then released below it; this typically happens in case of lamp replacement. After a re-lamp cycle, a new pre-heating sequence will be repeated.
3. This fault actually is a "board" fault so a lamp replacement is not effective to restart the ballast

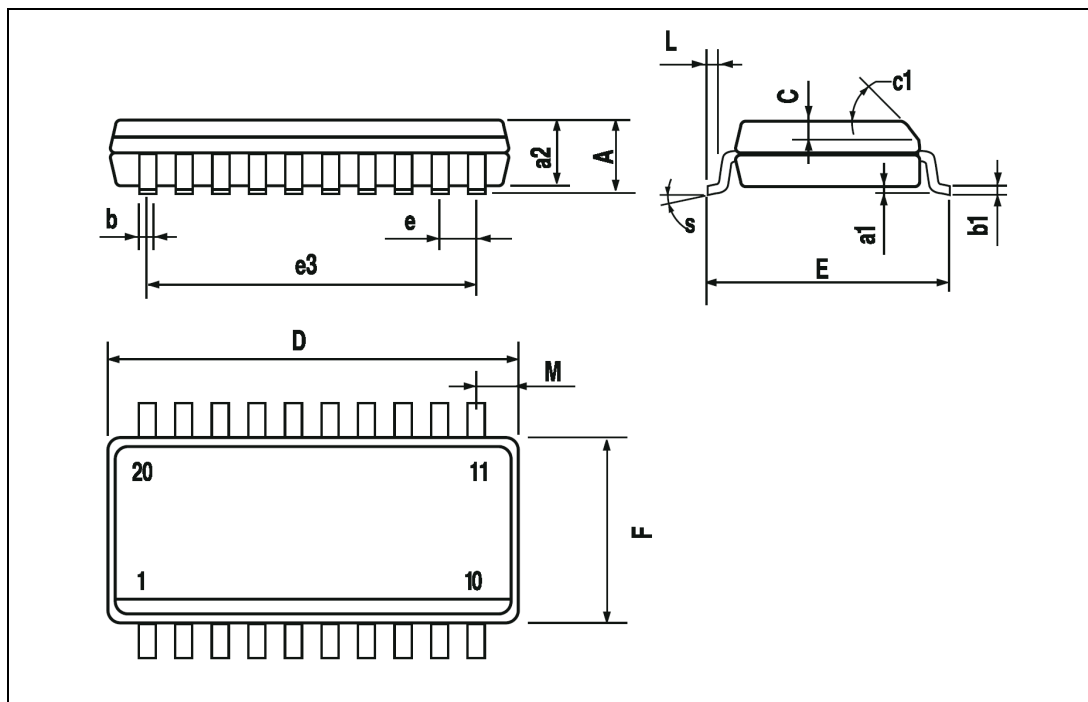
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8. SO-20 mechanical data

| Dimensions | | | | | | |
|------------|------------|-------|-------|-------|-------|-------|
| Ref. | mm. | | | inch | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |

Figure 7. Package dimensions



11 Order codes

Table 9. Order codes

| Part Number | Package | Packaging |
|--------------------|----------------|------------------|
| L6585D | SO-20 | Tube |
| L6585DTR | SO-20 | Tape and Reel |

12 Revision history

Table 10. Revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 12-Jan-2006 | 1 | Initial release |
| 25-Oct-2006 | 2 | Final datasheet |
| 21-Dec-2006 | 3 | Updated f_{RUN} value on Table 4: Electrical characteristics on page 8 |
| 12-Apr-2007 | 4 | Updated electrical values on Table 4 |
| 23-May-2007 | 5 | Updated Figure 1: Block diagram on page 1 and Eq.1 and 4 |

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